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# MS-7B33

ATX:226mm\*185mm

Ver: 10

## Intel -CoffeeLake-S plamform

### CPU:

LGA1151

CPU POWER PAK \*4Phase

GT POWER PAK \*2 Phase

### System Chipset:

Cannon Lake H310

### Onboard Chip:

SIO: NCT5567D colay NCT5565D

HD Audio Codec: ALC887

LAN: RTL8111H

Flash ROM: SPI 64 MB

DP to VGA: RTD2167

CUT VBAT:SLG4B41231

### PWM:

VCORE - RT3607

DDR - RT8231

DDR VPP25- MP2143

PCH(1.05V) - RT8125E

VCCSA - RT8125E

VCCIO - MP5077(Load Switch)

### Main Memory:

DDR4 \* 2 (Dual Channel)

### ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8\_VSB:GS7133

3VDSW:GS7116

VCCSTPLL:GS7133

### Expansion Slots:

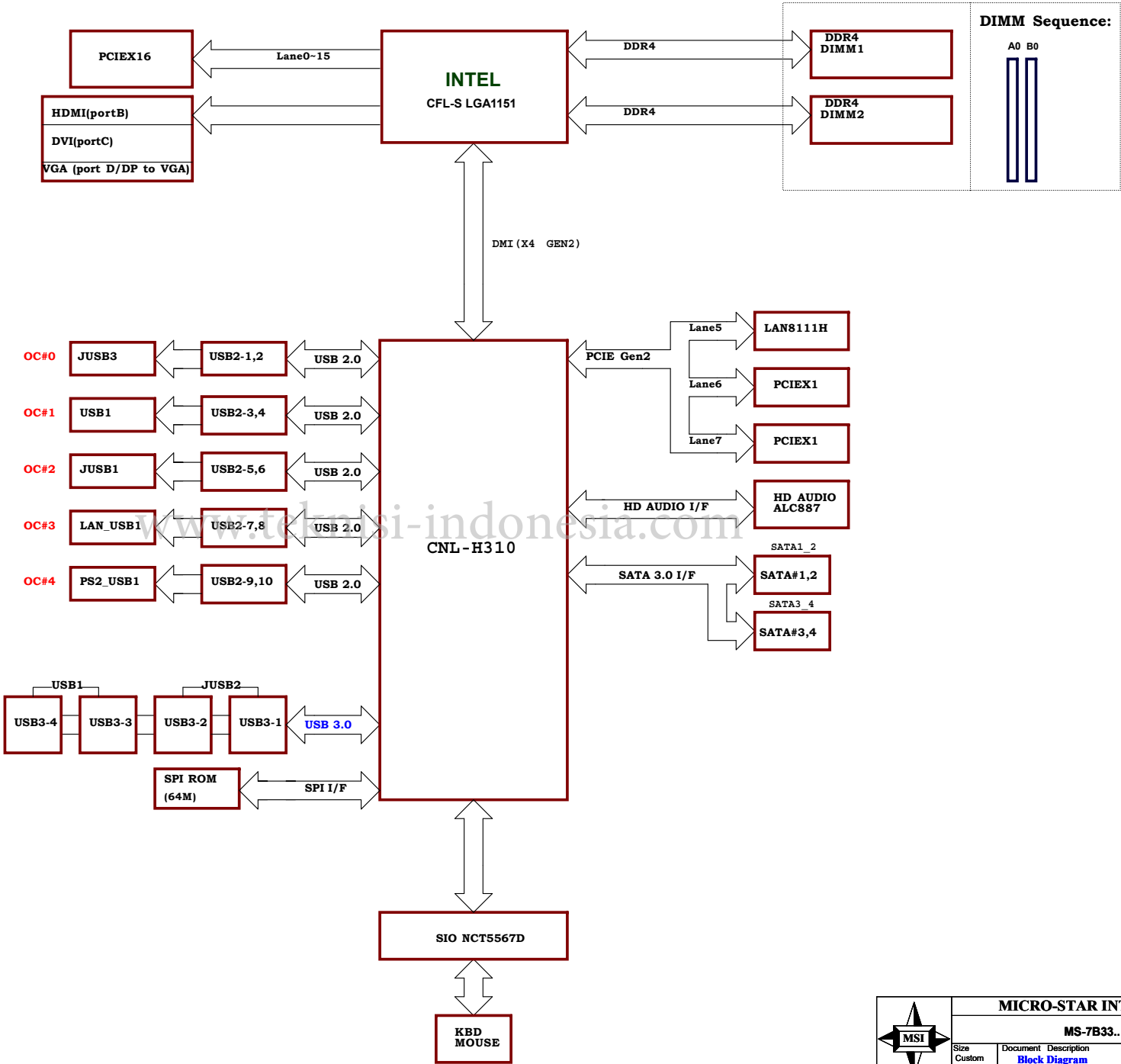
PCI Express (X16) Slot \* 1

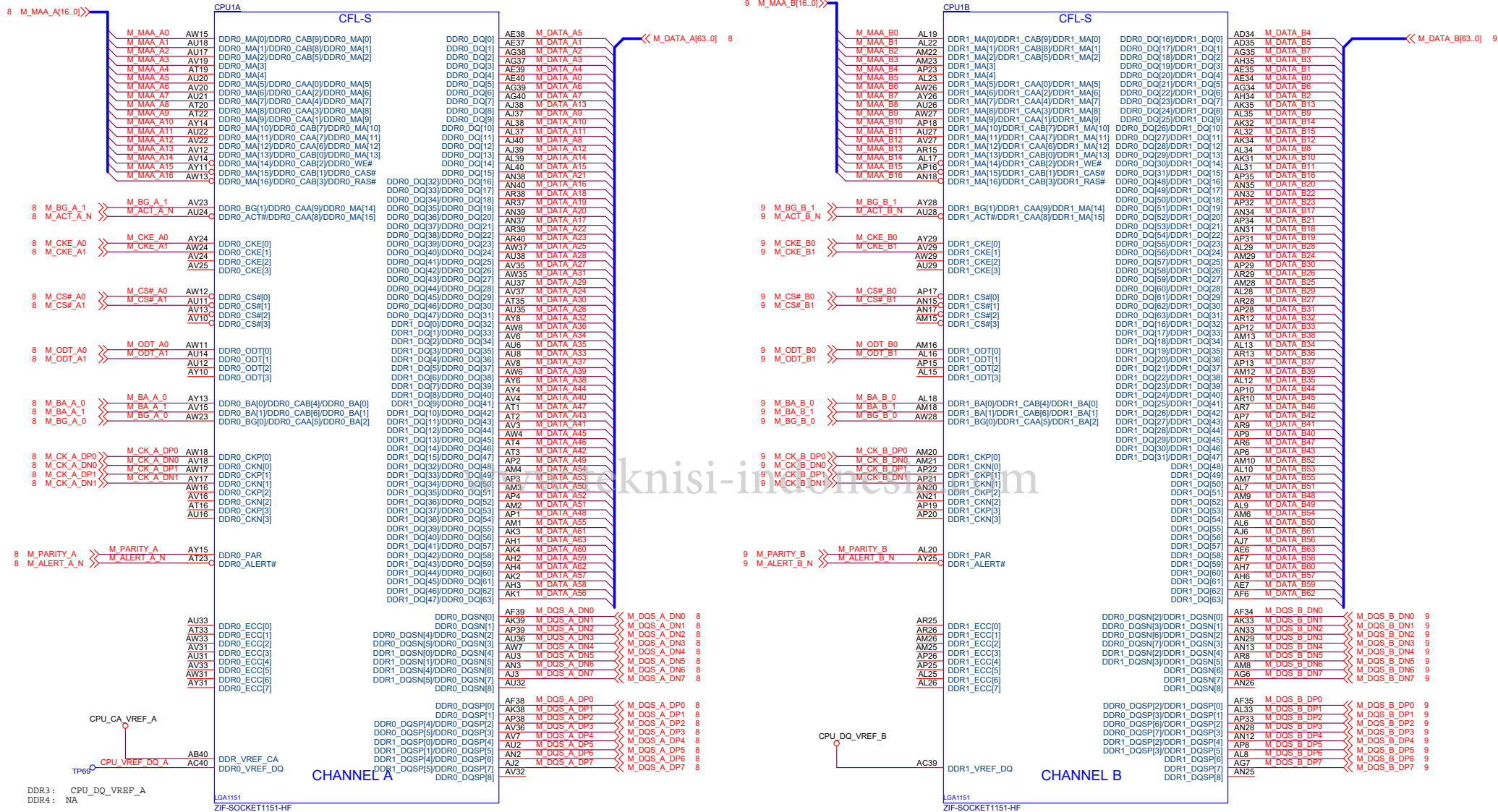
PCI Express (X1 ) Slot \* 2



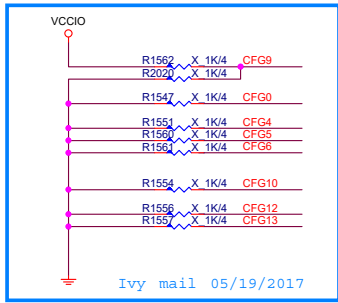
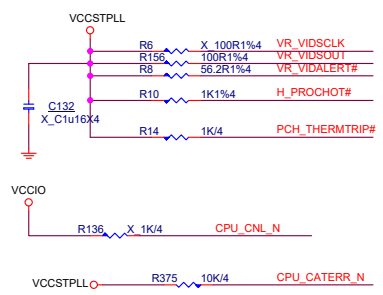
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MS-7B33 Block Diagram

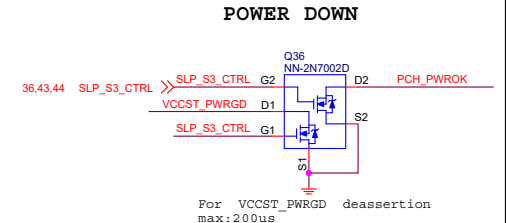
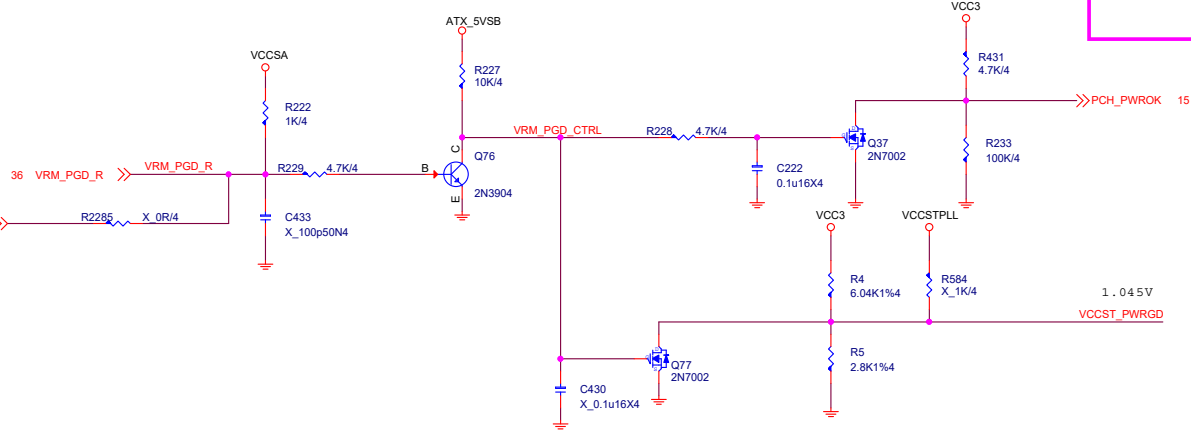
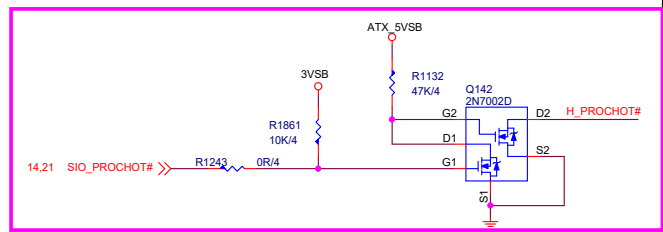
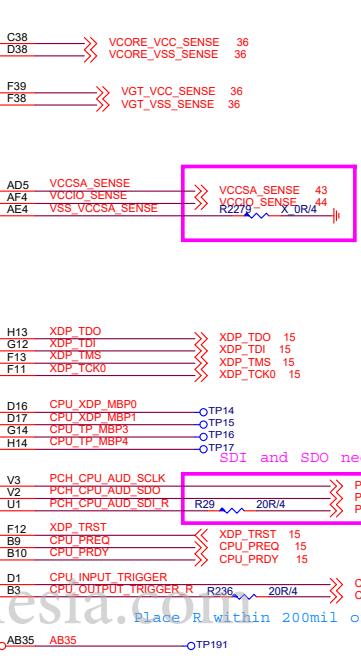
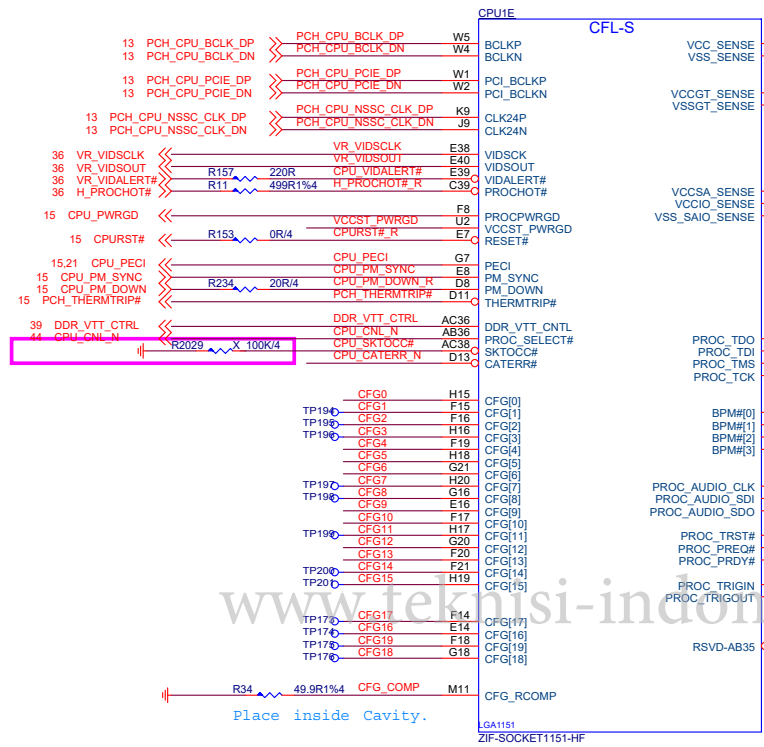




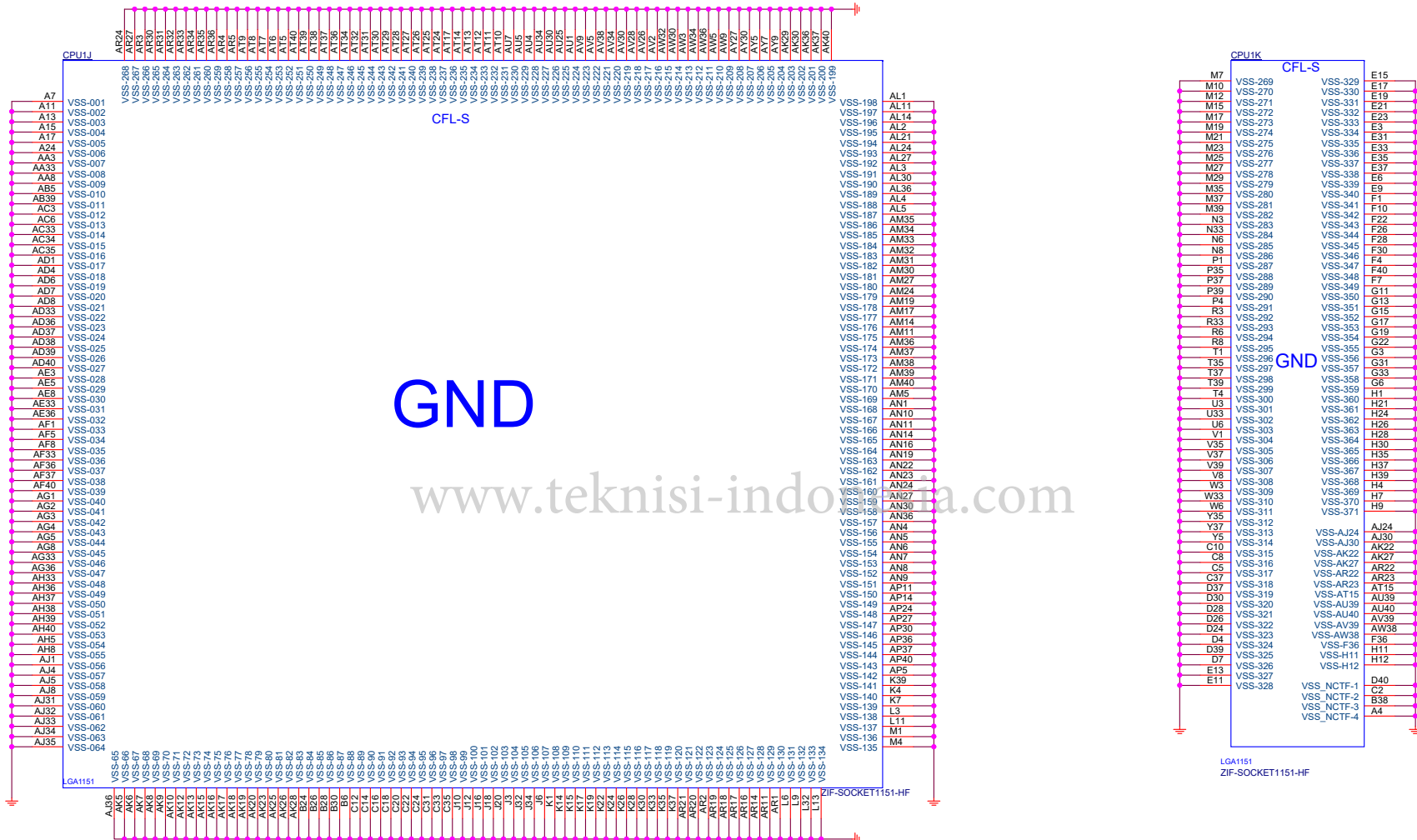




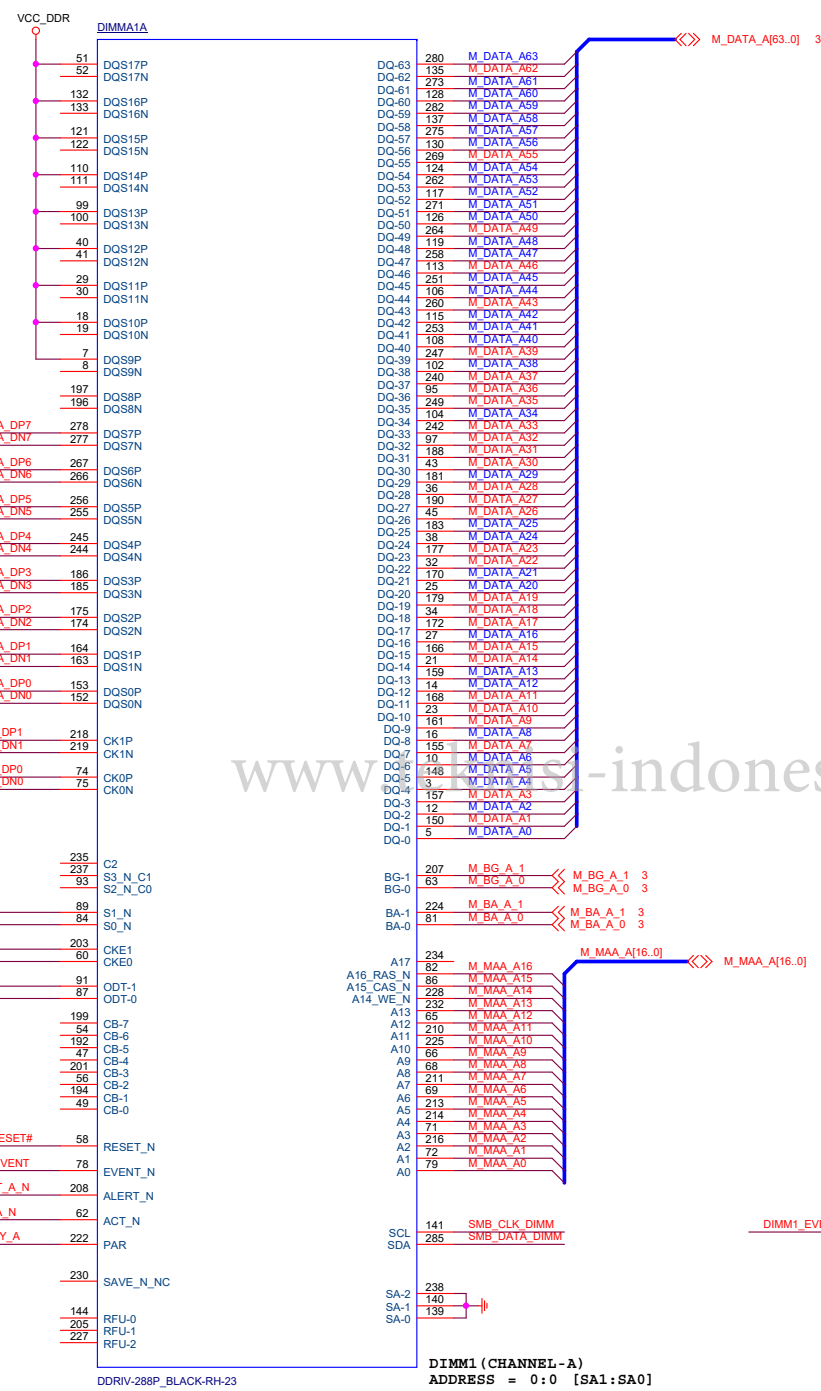
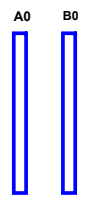
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1		RSVD	RSVD
2	NORM	REVERSE	FB3 LANE REVERSAL
3		RSVD	RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	FB3CFGSEL[0]
6	DISABLE	ENABLE	FB3CFGSEL[1]
7	RESET#	BIOS REQ	FB3 DEFER TRAINING
8		RSVD	RSVD
9		RSVD	RSVD
10		RSVD	RSVD
11		RSVD	RSVD
12		RSVD	RSVD
13		RSVD	RSVD
14	RSVD		RSVD
15	RSVD		RSVD





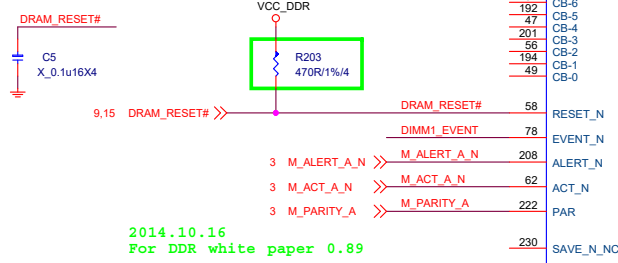




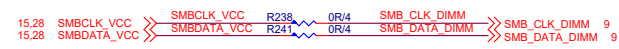


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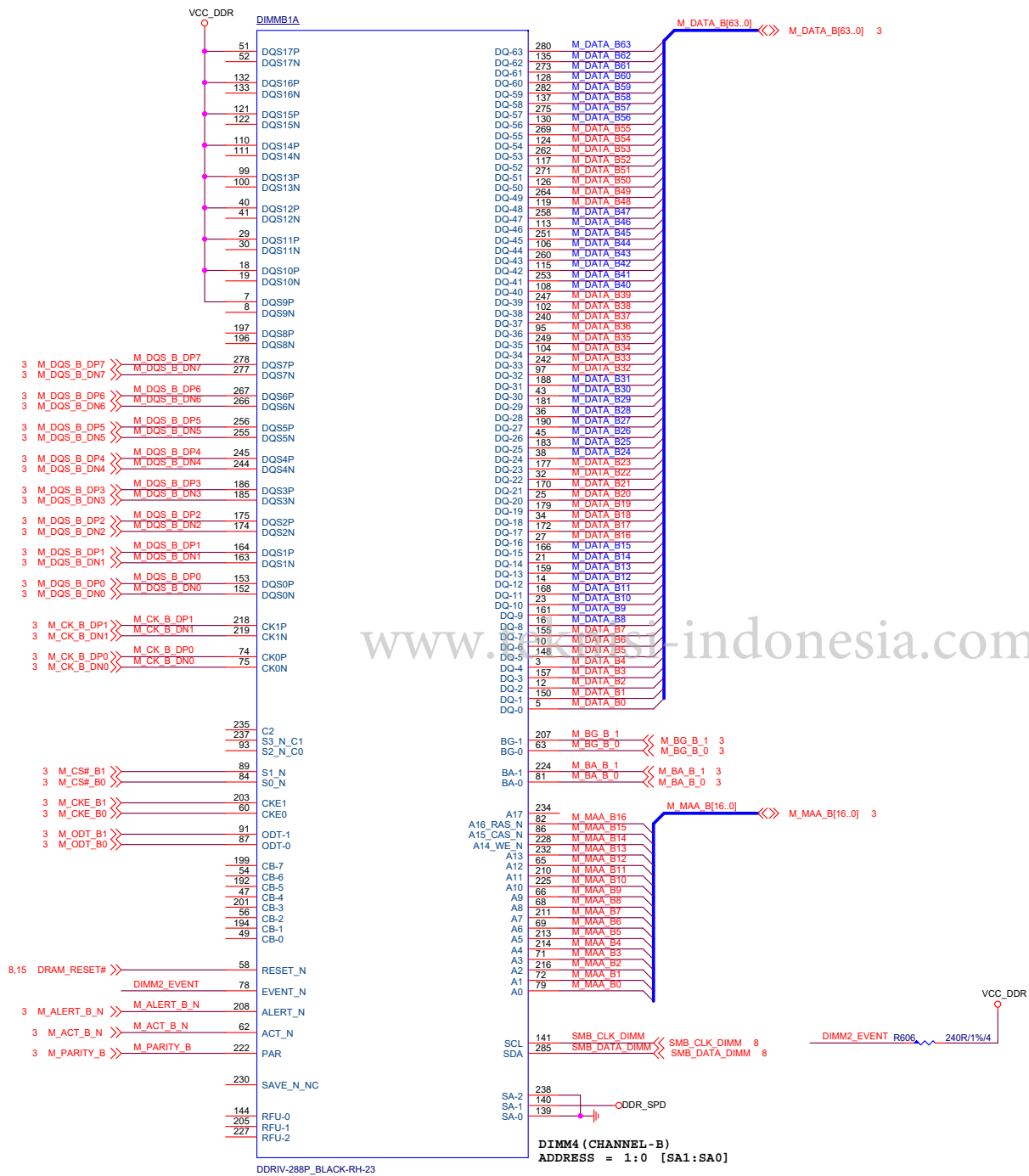
2014.10.16  
For DDR white paper 0.89



DIMM1 (CHANNEL - A)  
ADDRESS = 0:0 [SA1:SA0]

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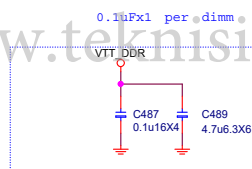
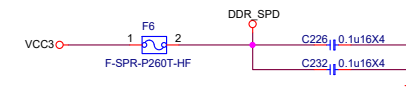


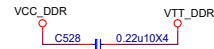
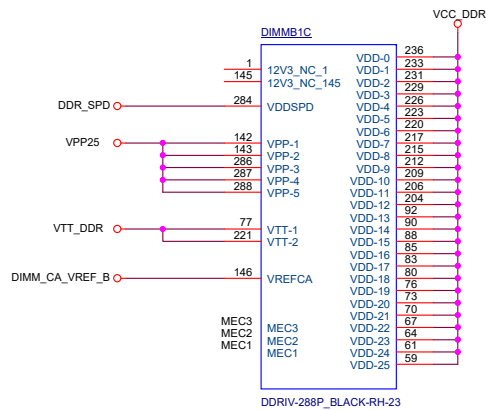


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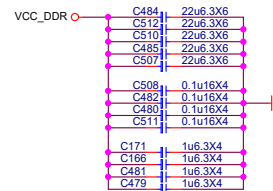
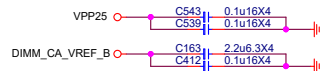
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Custom	DDR4 DIMM 2		10
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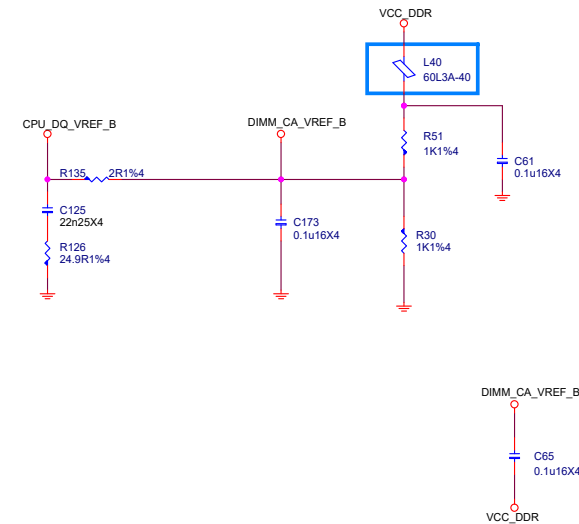
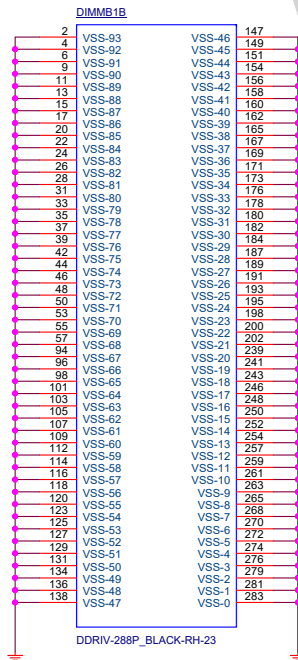
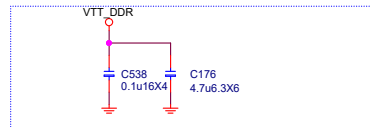


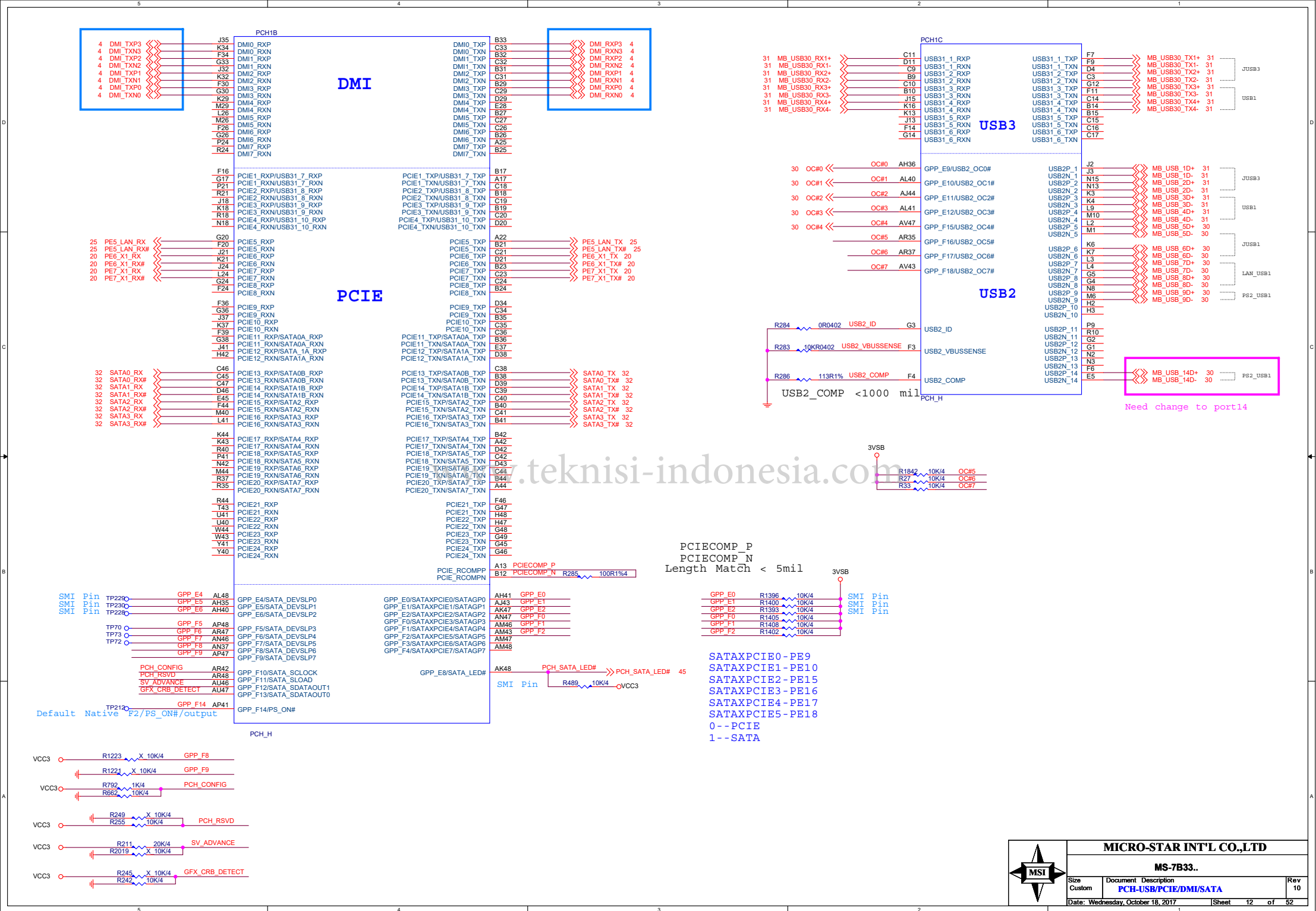
Place close to DIMM2



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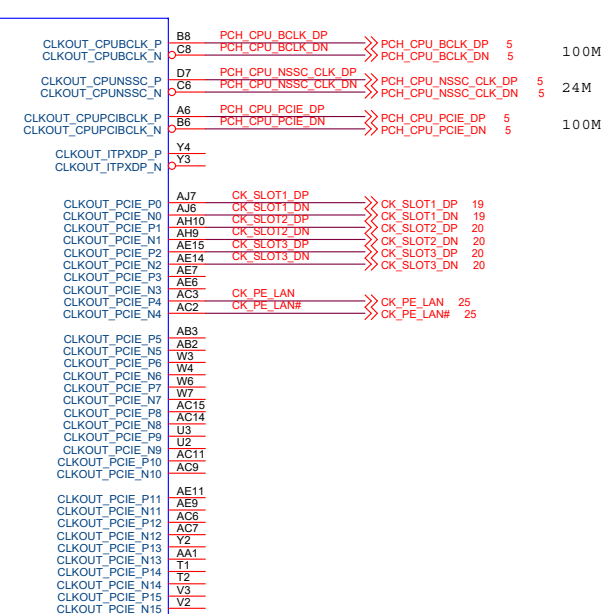
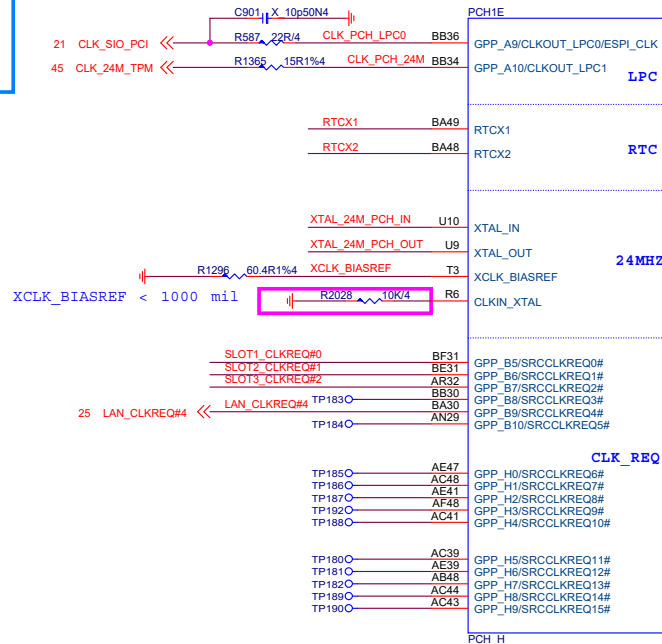
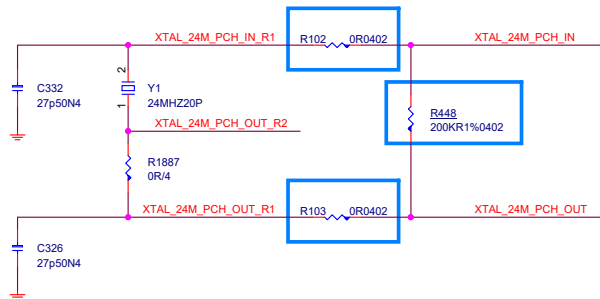
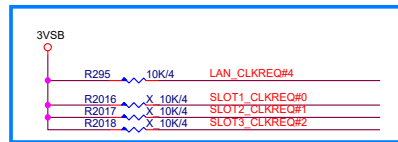
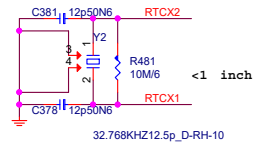
0.1uFxl per dimm



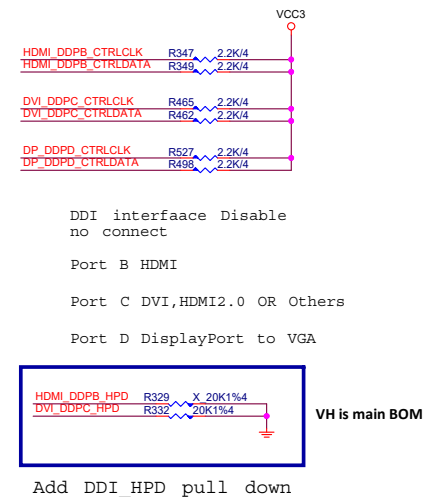
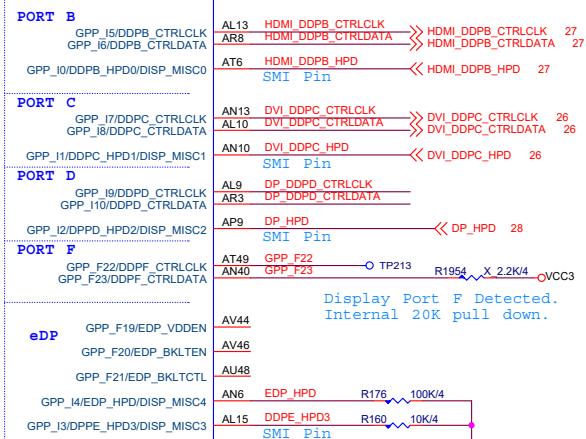
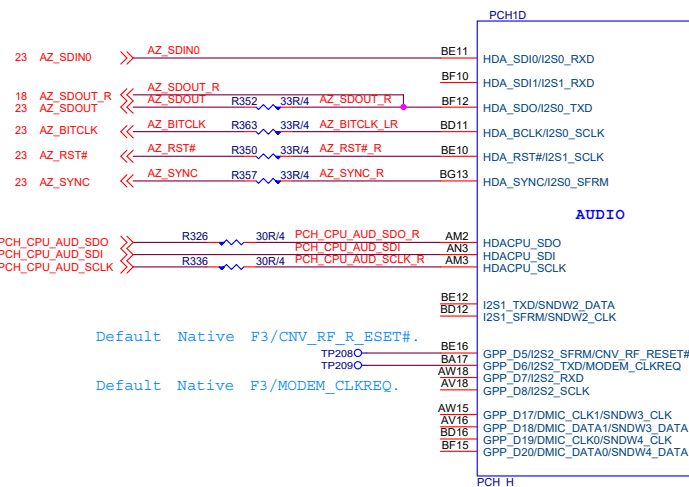
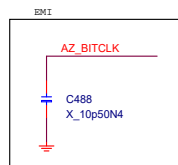


Close to PCH

Close to PCH



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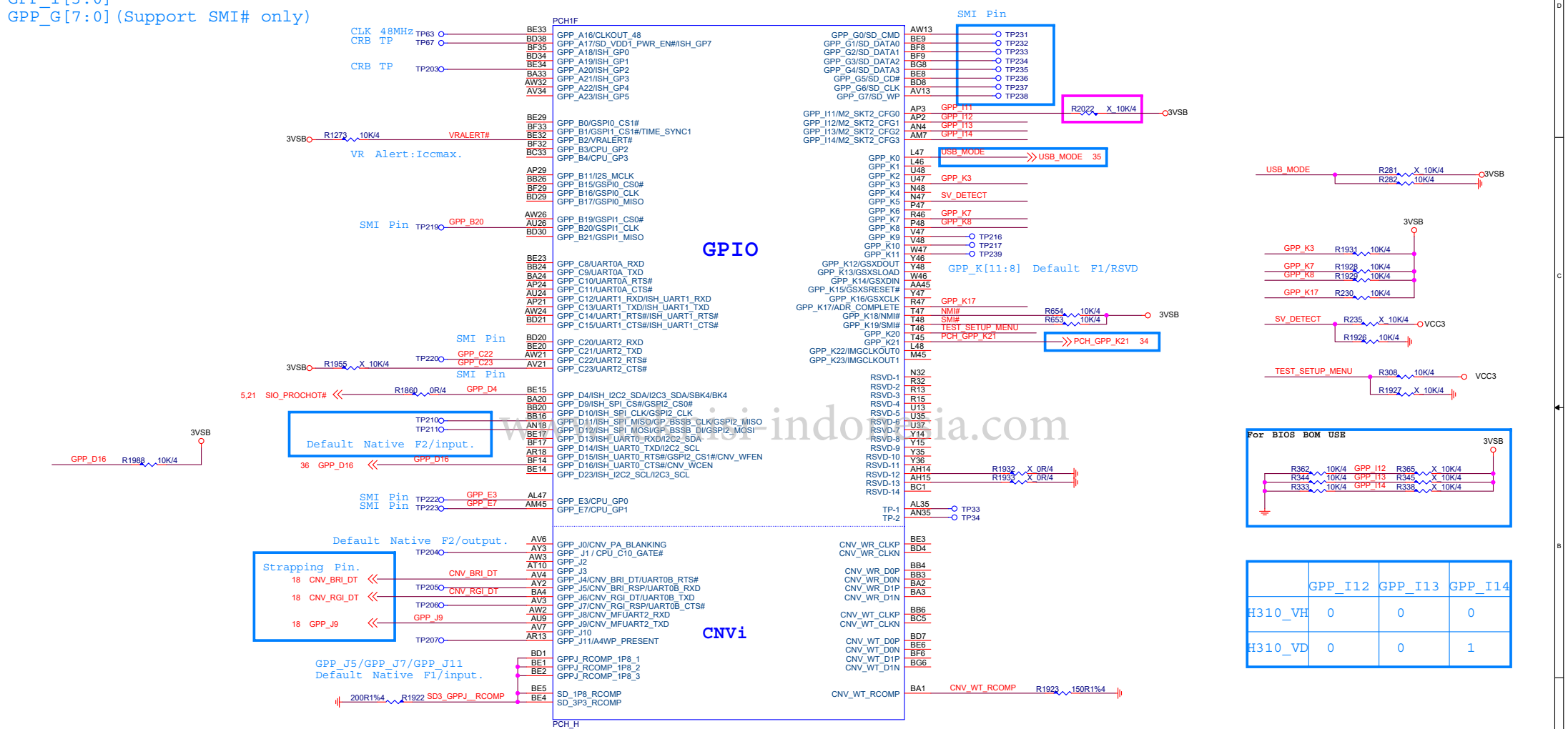


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**MS-7B33..**

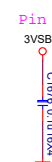
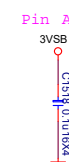
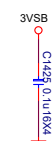
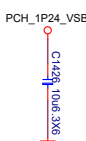
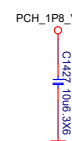
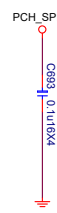
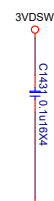
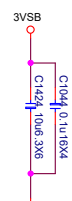
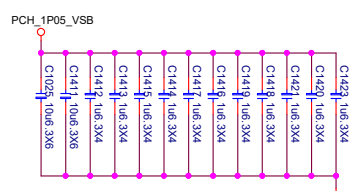
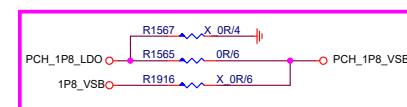
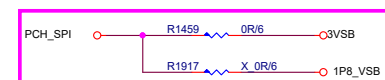
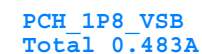
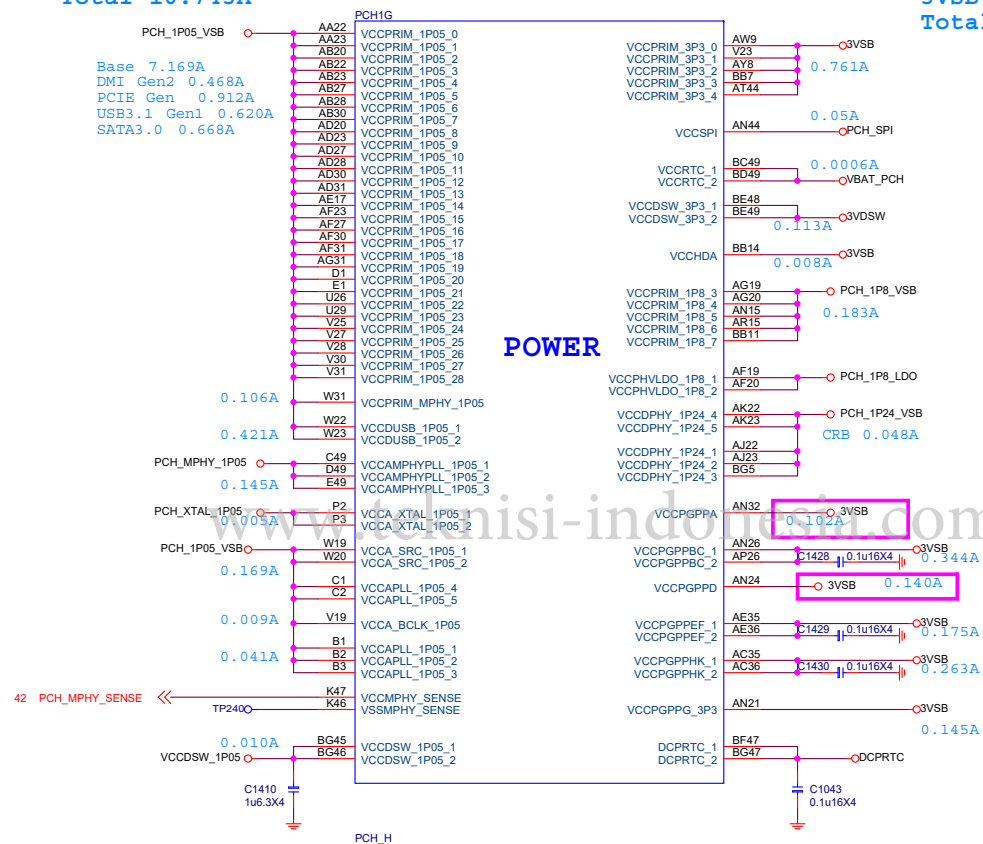
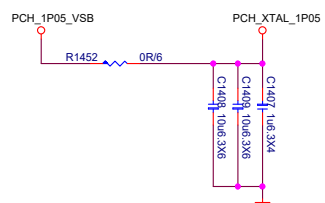
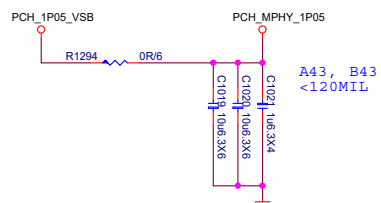
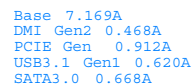
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GPIO (SMI/NMI) :  
GPP\_B14,GPP\_B20,GPP\_B23  
GPP\_C[23:22]  
GPP\_D[4:0]  
GPP\_E[8:0]  
GPP\_I[3:0]  
GPP\_G[7:0] (Support SMI# only)



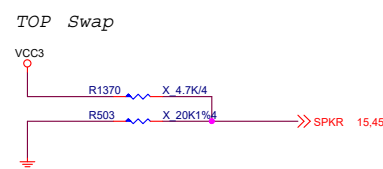
Custom		FCH-LPC/SPI/SMBUS/MISC		10
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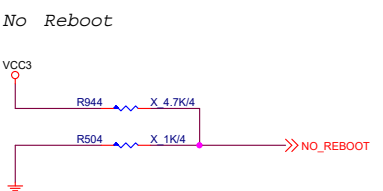


VSS

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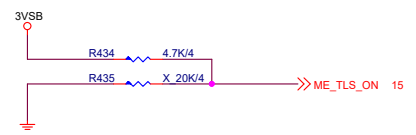
Internal pull-down 20K is disabled after PLTRST#



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

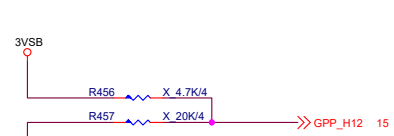
AMT and SBA with confidentiality



0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

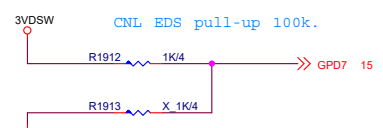
ESPI FLASH SHARING MODE



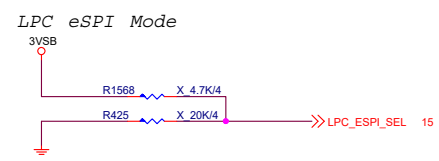
0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

Reserved



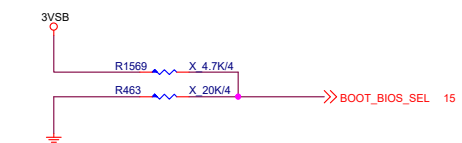
XTAL INPUT MODE  
0 = XTAL INPUT IS SINGLE-ENDED  
1 = XTAL INPUT IS DIFFERENTIAL  
PCH HAS INTERNAL 20K PD



0 : LPC  
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

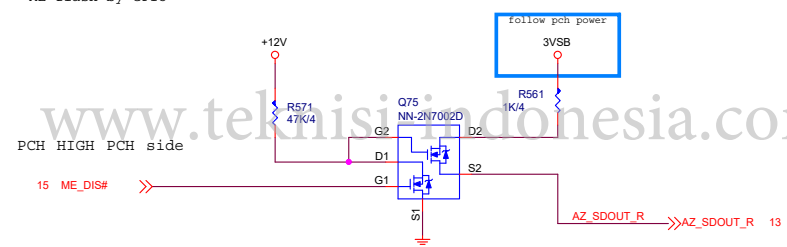


0 : SPI  
1 : LPC

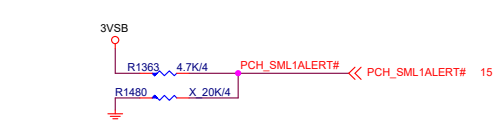
Internal pull-down 20K is disabled after PLTRST

HDA\_SDO

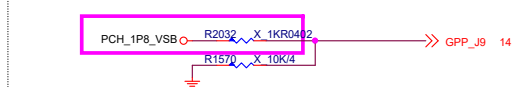
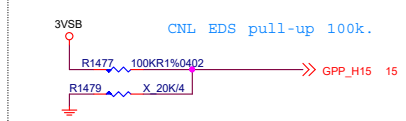
ME flash by GPIO



Reserved

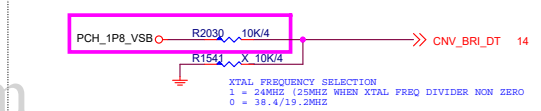


Reserved

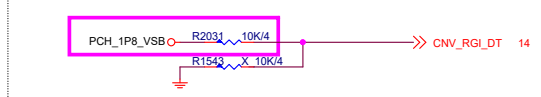


VCCSPI 3.3V, Internal pull-down.

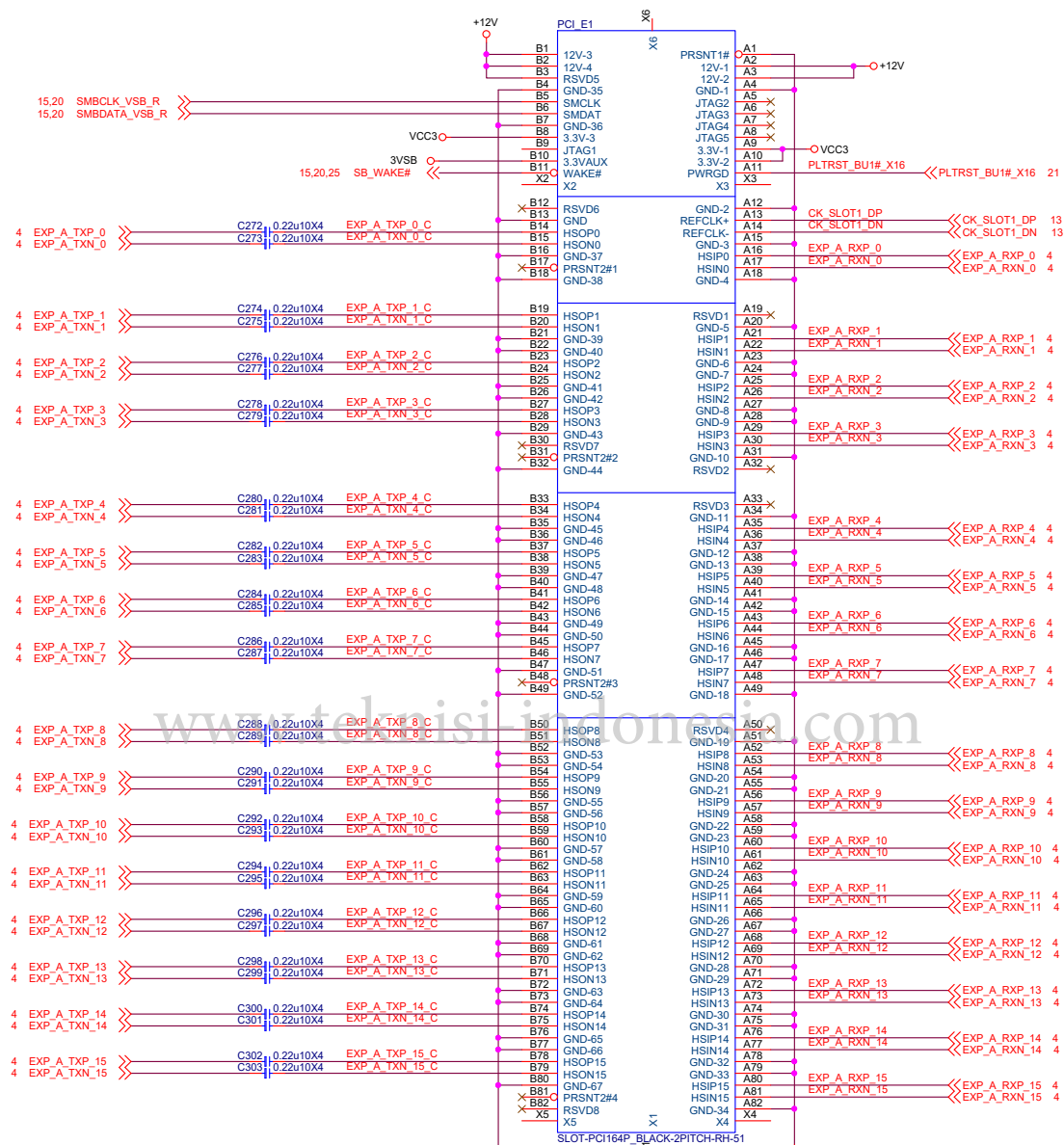
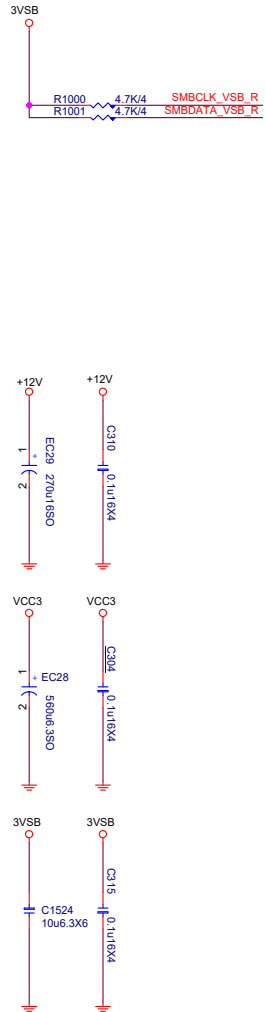
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE  
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT  
1 = VCCSPI IS CONNECTED TO 1.8V RAIL  
PCH HAS INTERNAL 20K PD

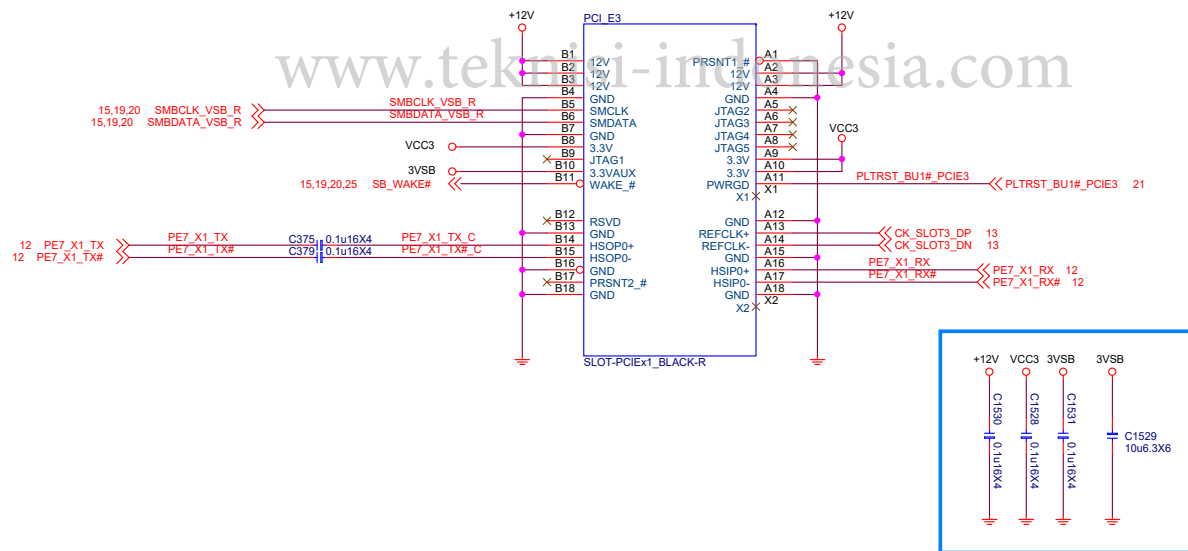
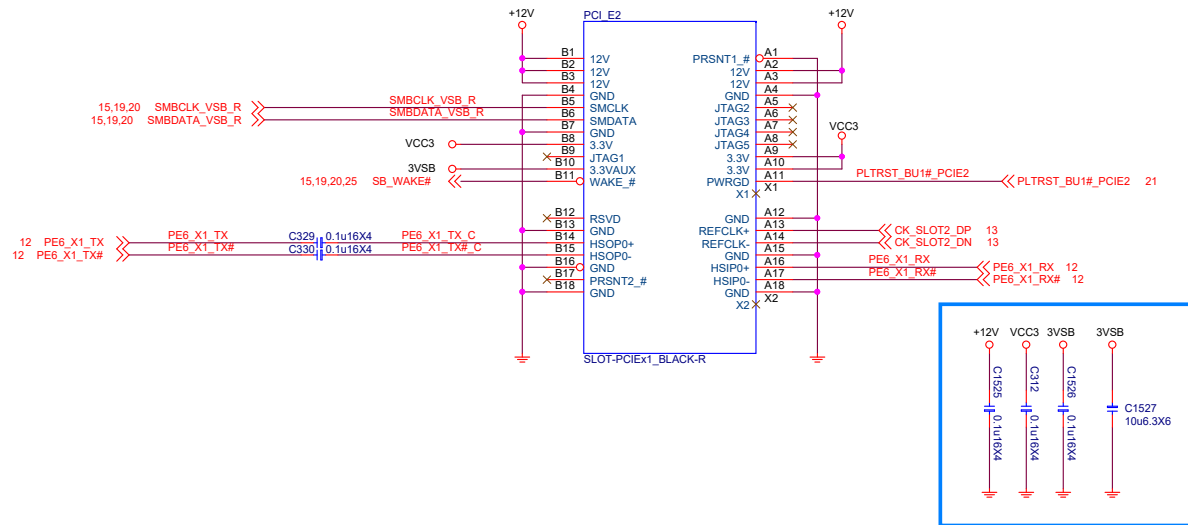


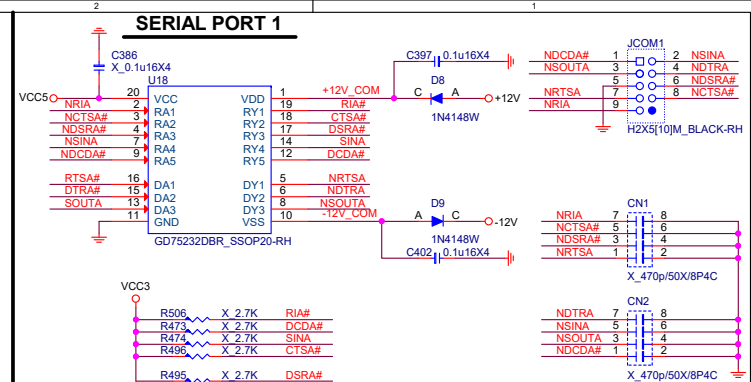
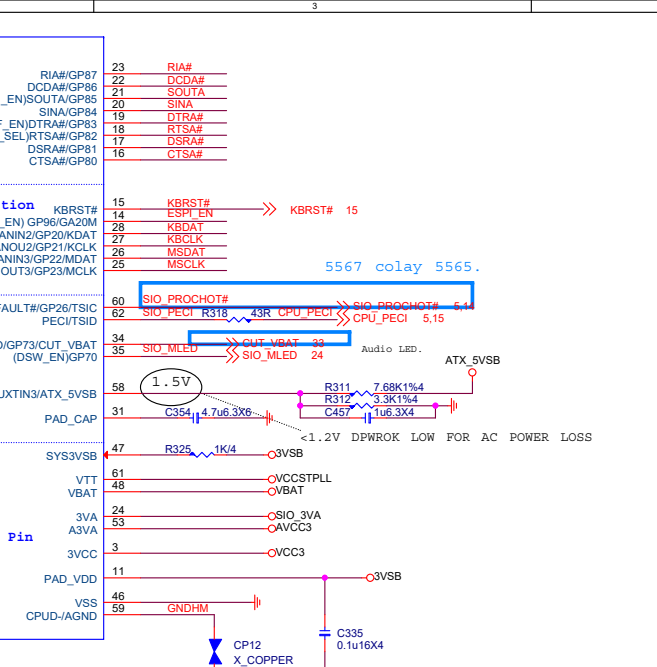
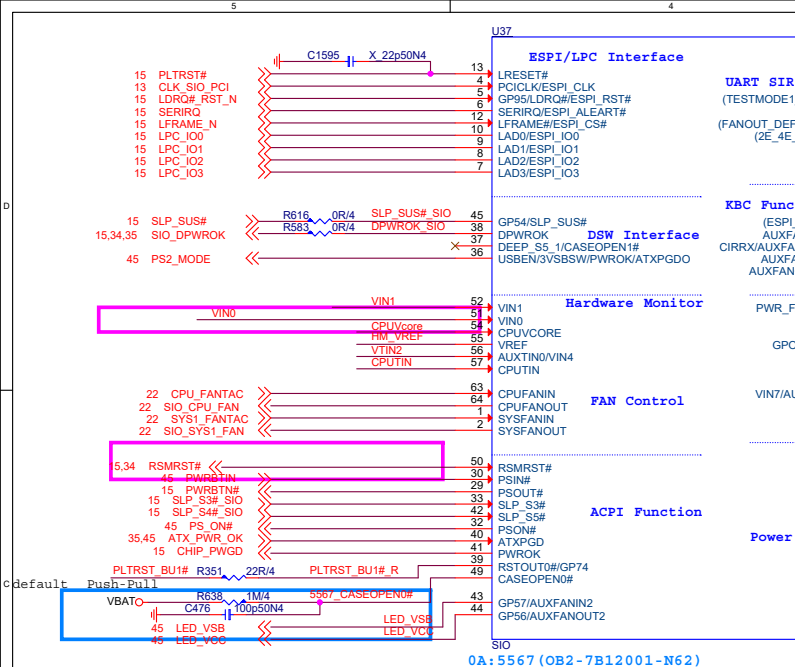
XTAL FREQUENCY SELECTION  
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO  
0 = 38.4/19.2MHZ



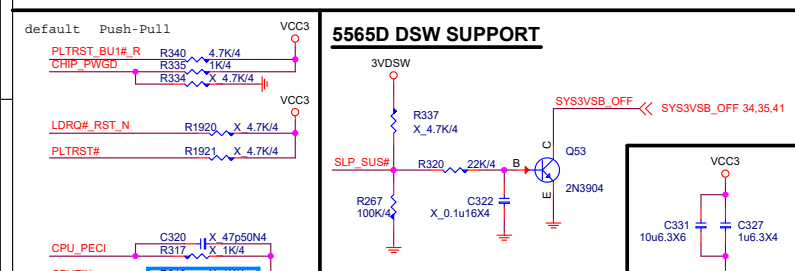
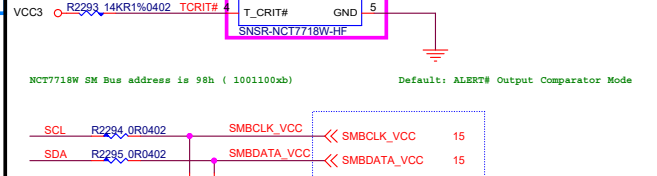
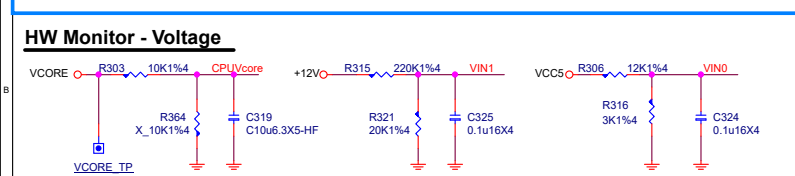
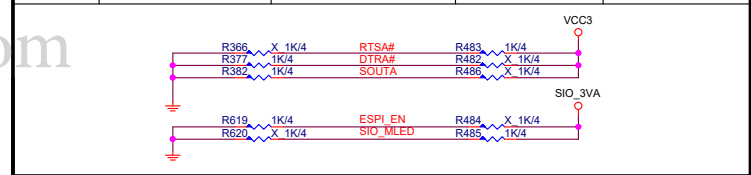
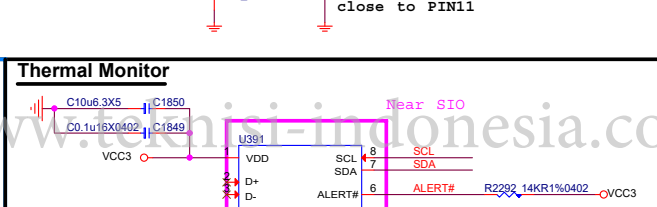
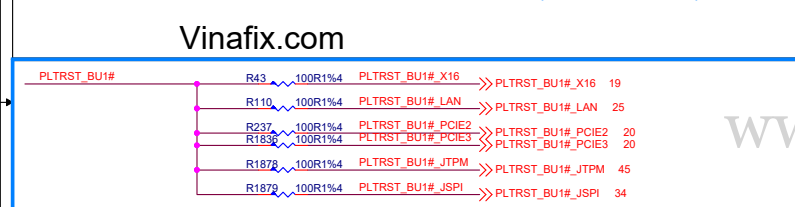
CNL EDS  
0 = Integrated CNVi enable  
1 = Integrated CNVi disable



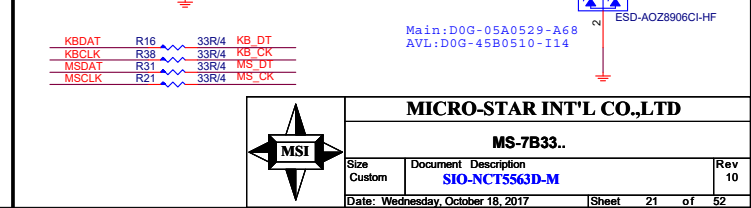
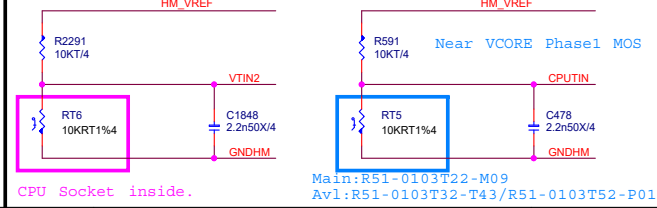
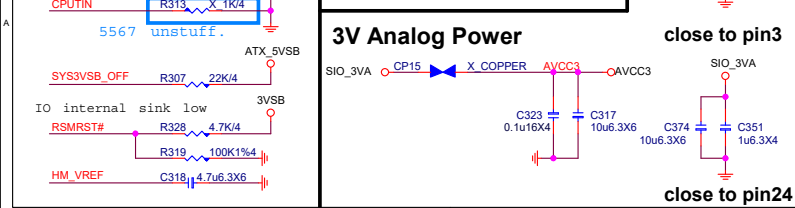
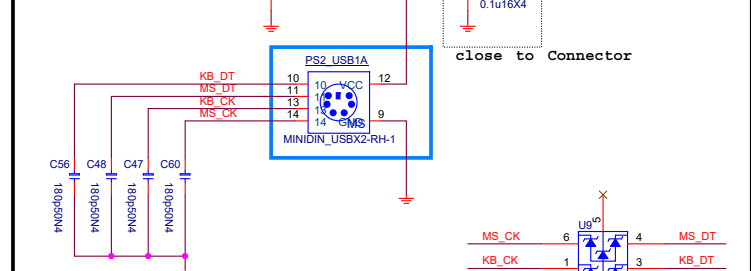




PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TESTMODE	ENABLE TESTMODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN



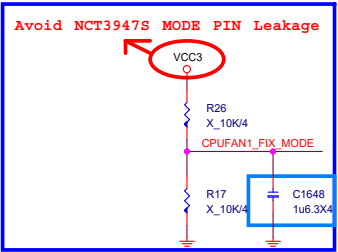
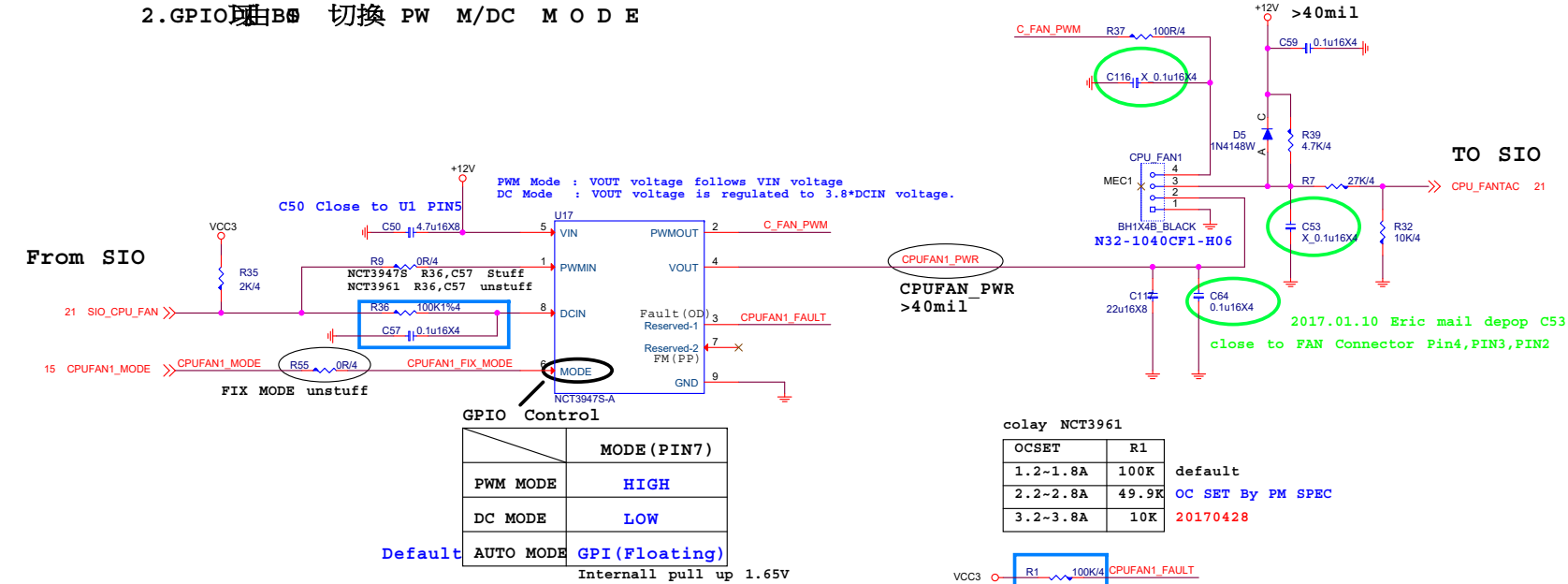
TEMPERATURE (°C)	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
2KΩ	77	87	97	107	117
7.5KΩ	79	89	99	109	119
10.5KΩ	81	91	101	111	121
14KΩ	83	93	103	113	123
18.7KΩ	85	95	105	115	125



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MS-7B33..			
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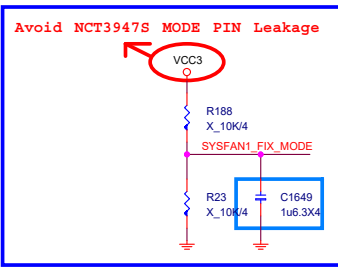
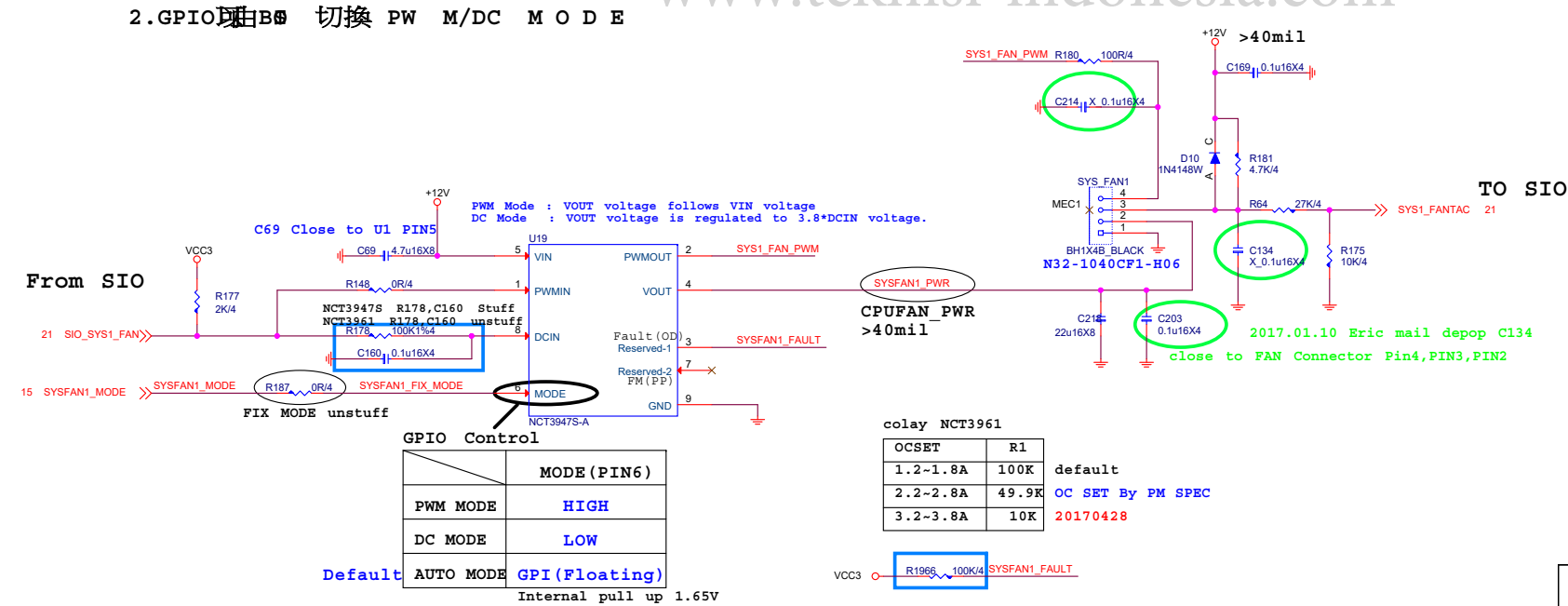
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO 1.65V 切换 PW M/DC M O D E



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO 1.65V 切换 PW M/DC M O D E



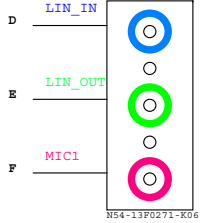
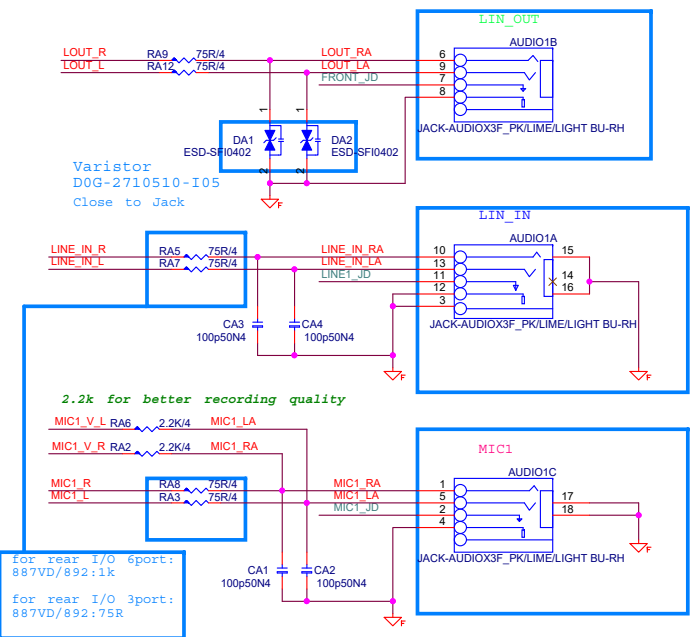
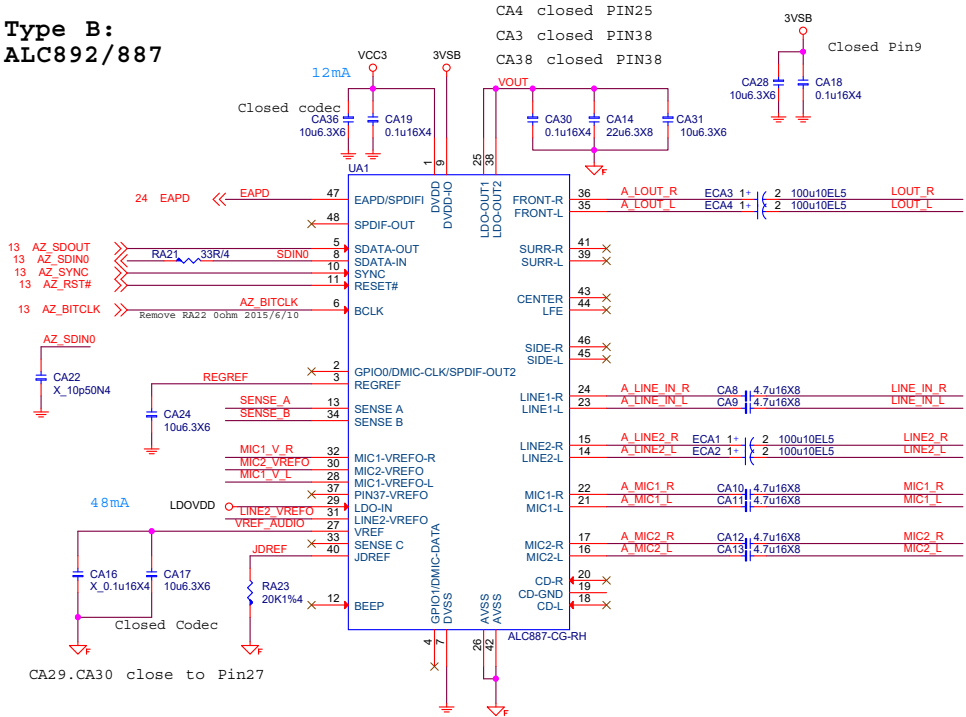
MICRO-STAR INT'L CO.,LTD

MS-7B33..

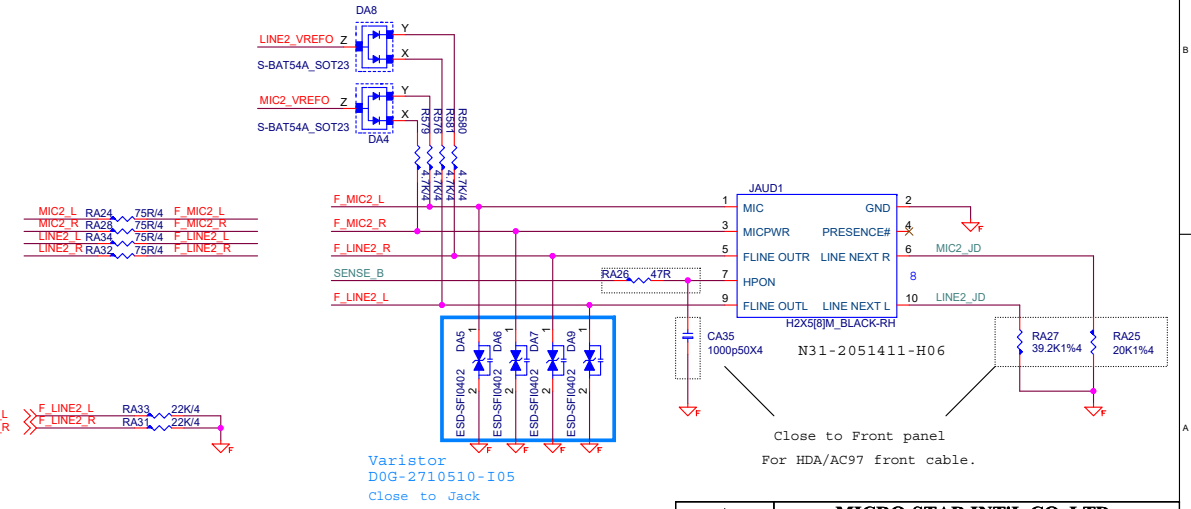
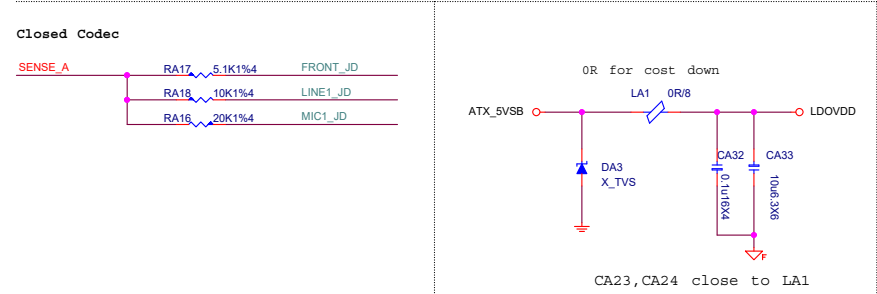
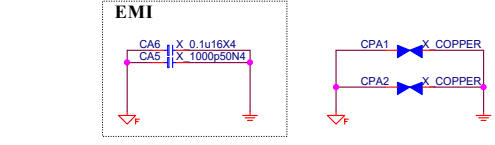
Size	Document	Description	Rev
Custom		FAN CONTROLLER	10
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Type B:  
ALC892/887

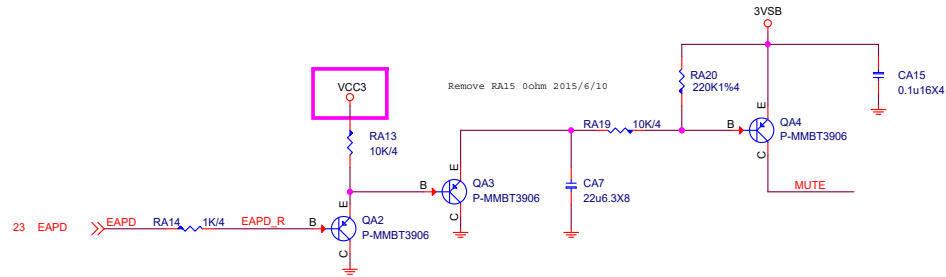


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## Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

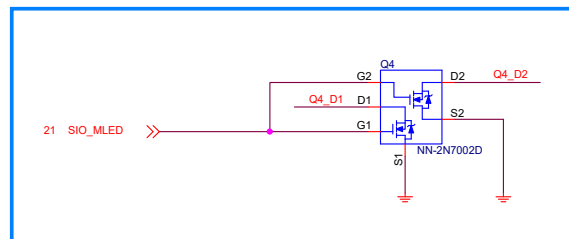
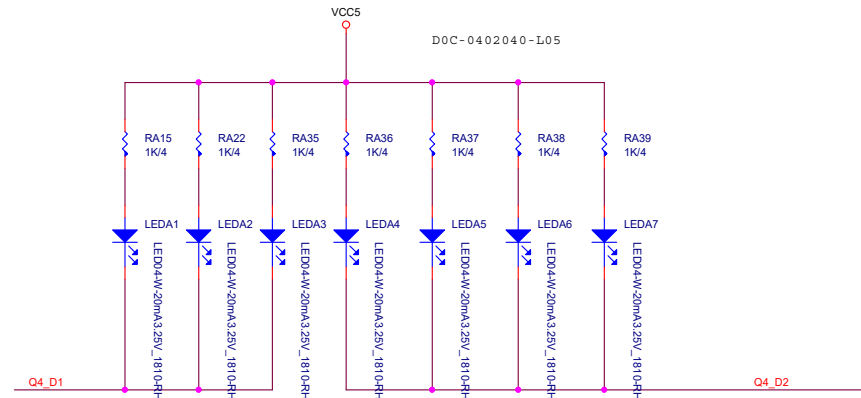
Vinafix.com

Digital

Analog



## Audio LED



2016.01.12:Modify Q4 to Dual 7002 & Remove 0R

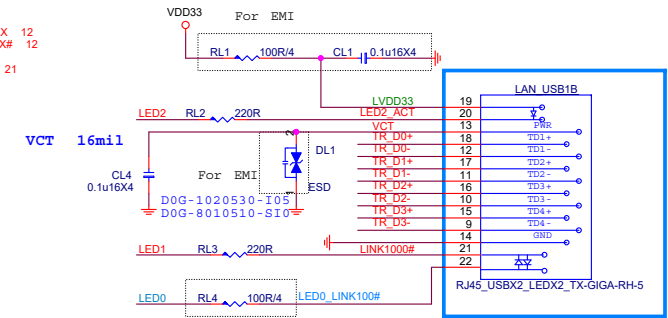
MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7B33..			
Size	Document	Description	Rev
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# RTL8111G/RTL8111H Giga LAN

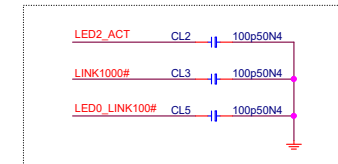
8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

LAN\_CLKREQ#4\_R R1014 0R/4 >>> LAN\_CLKREQ#4 13

## LAN Connector

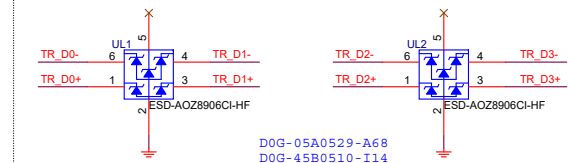


For EMI



## ESD Protect

UL1 & UL2 close to connector



D0G-05A0529-A68  
D0G-45B0510-I14

Pin33: 4 via from top layer to GND layer  
and make the via at the center of IC.

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## 8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

## 8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



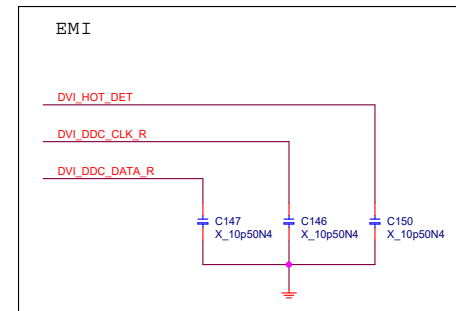
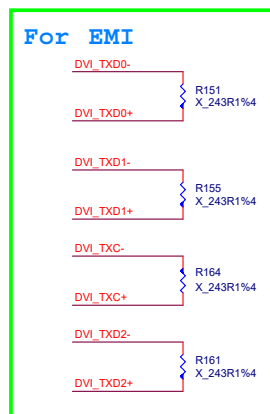
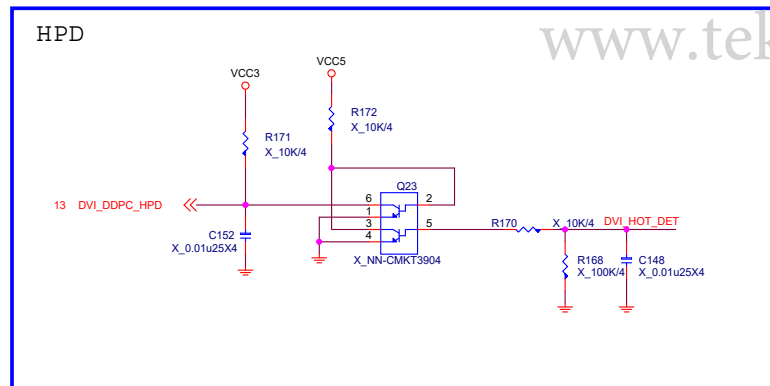
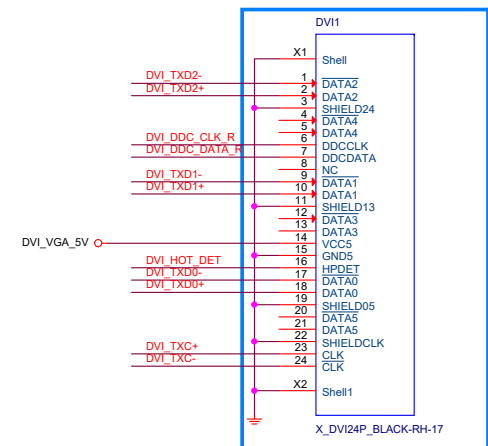
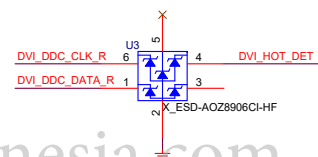
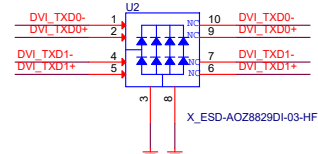
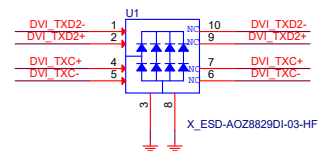
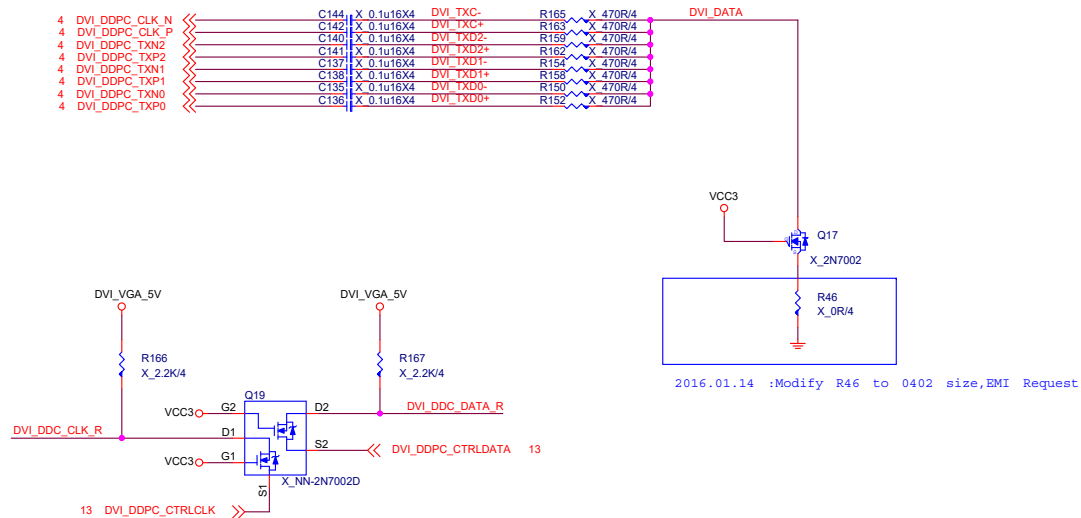
MICRO-STAR INT'L CO.,LTD

MS-7B33..

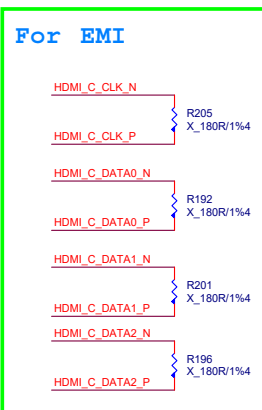
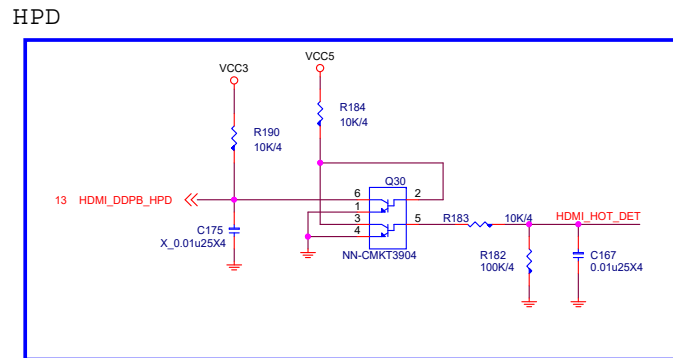
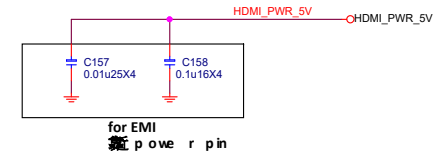
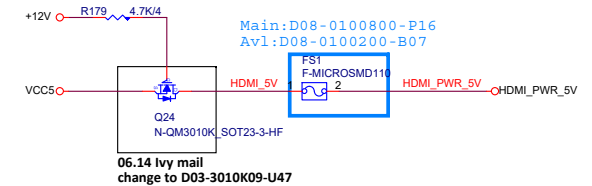
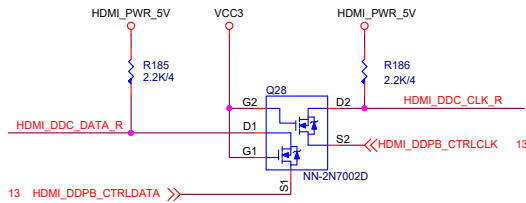
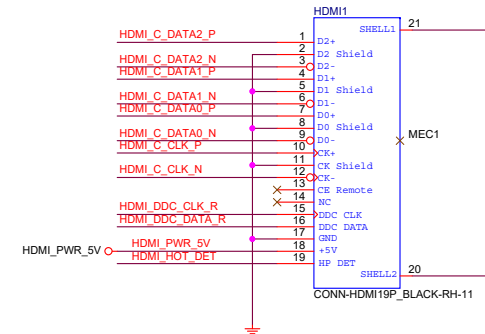
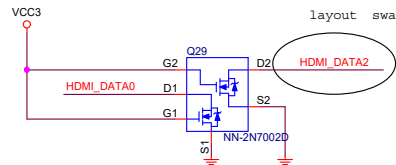
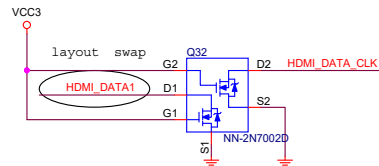
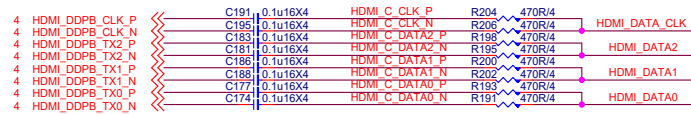
Size	Document	Description	Rev
Custom		LAN - RTL8111H	10
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# DVI level shifter

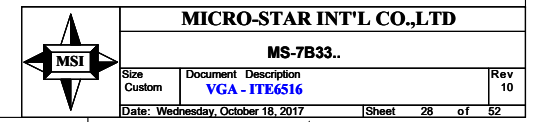
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)




HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



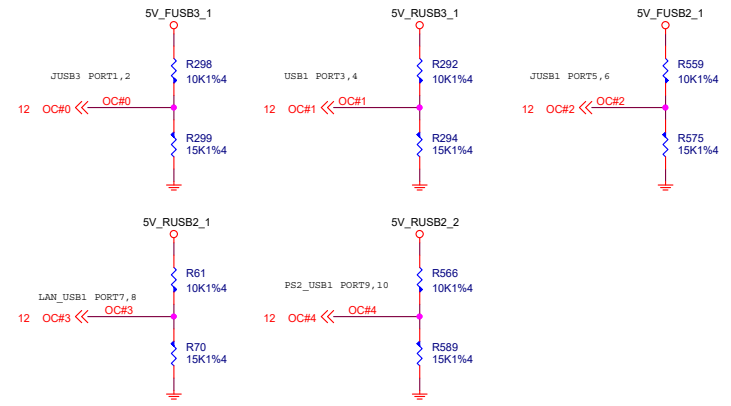
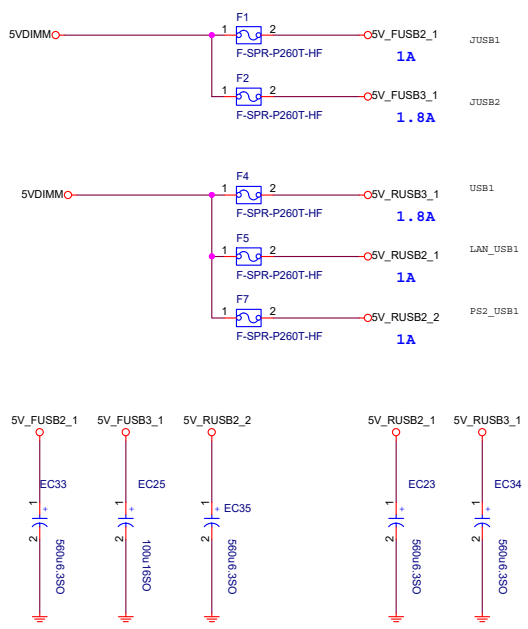
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



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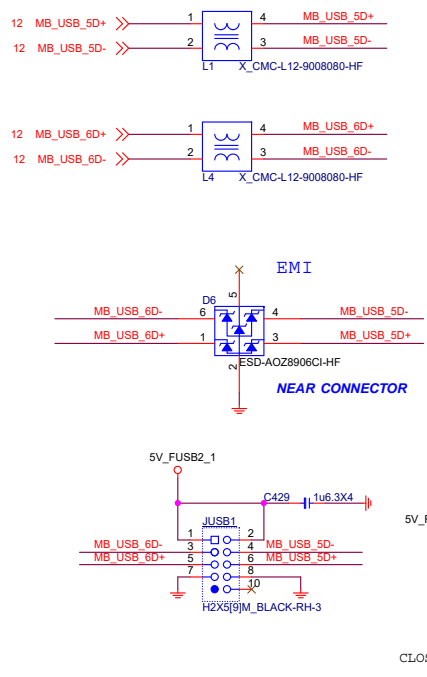
	MICRO-STAR INT'L CO.,LTD	
	MS-7B33..	
Size Custom	Document Description <b>M.2-SLOT1</b>	Rev 10
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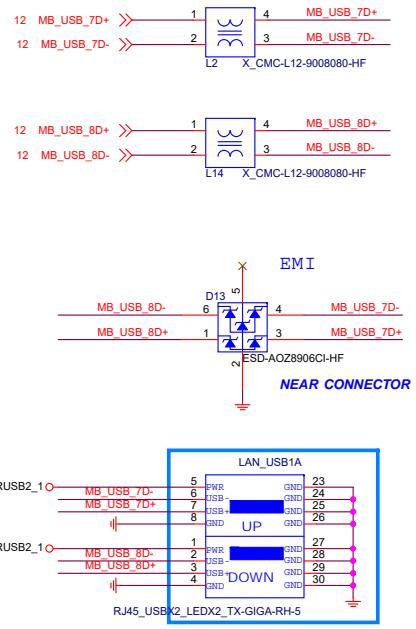
USB CONN	USB POWER	PCB PORT	OC# SIGNAL
JUSB1	5V_FUSB2_1	Port5,6	OC#2
PS2_USB1	5V_RUSB2_2	Port9,14	OC#4
JUSB3	5V_FUSB3_1	Port1,2	OC#0
USB1	5V_RUSB3_1	Port3,4	OC#1
LAN_USB1	5V_RUSB2_1	Port7,8	OC#3

### FRONT JUSB2 PORT 5,6

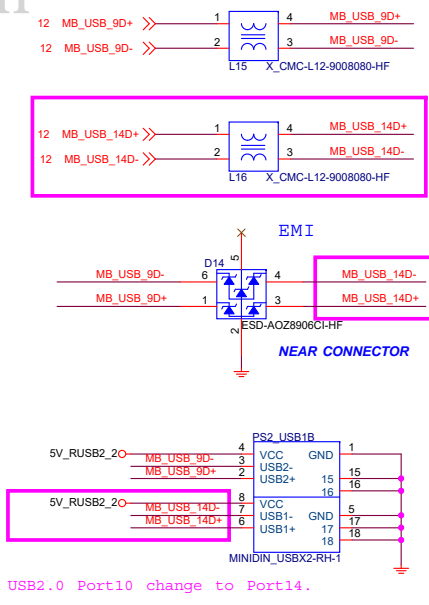


### USB1 PORT 7,8

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### FRONT PS2\_USB1 PORT 9,10



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**MS-7B33..**

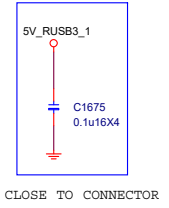
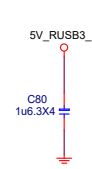
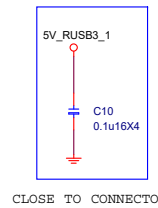
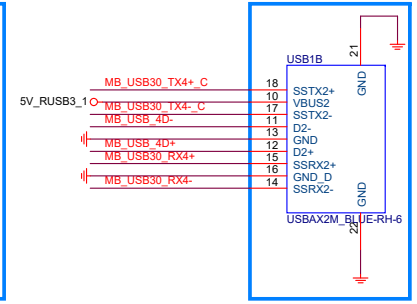
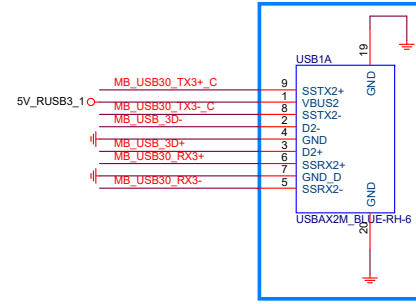
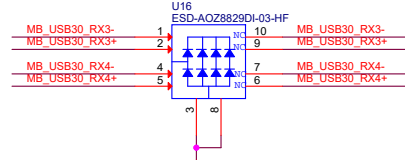
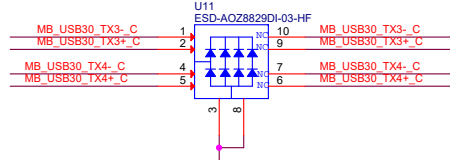
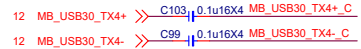
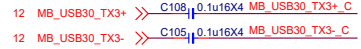
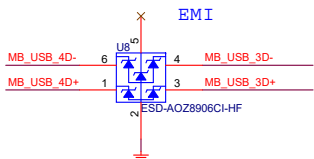
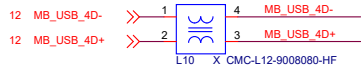
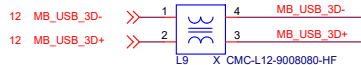
Size Custom	Document Description	Rev 10
Date: Wednesday, October 18, 2017	<b>USB2.0 Connector</b>	

CLOSE TO CONNECTOR

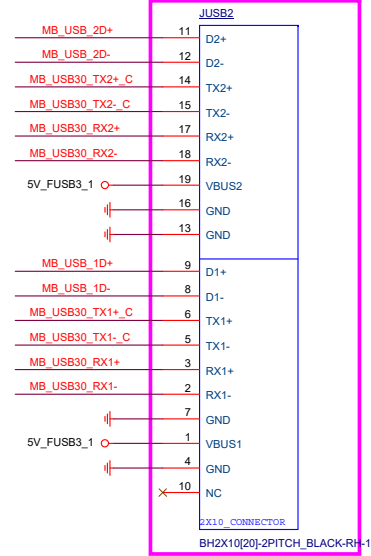
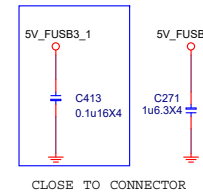
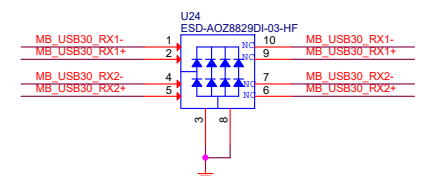
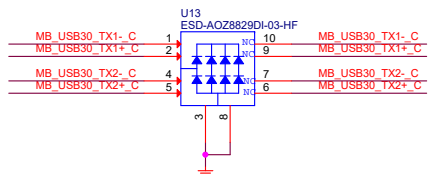
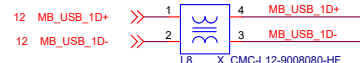
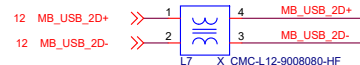
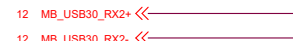
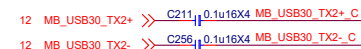
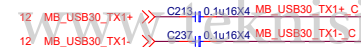
USB2.0 Port10 change to Port14.

CLOSE TO CONNECTOR

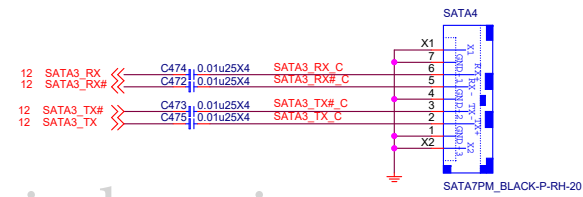
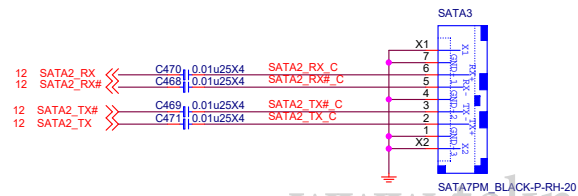
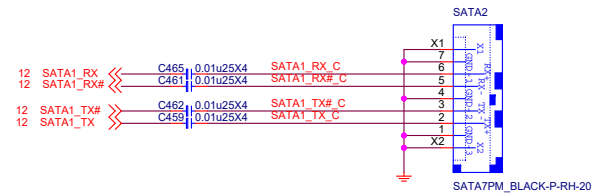
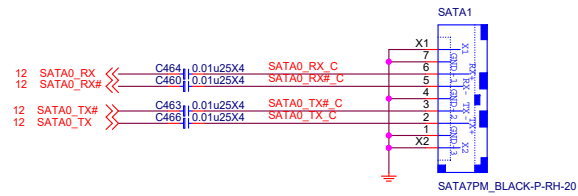
## Rear USB1 port 9,10



## Front JUSB3 port 1,2



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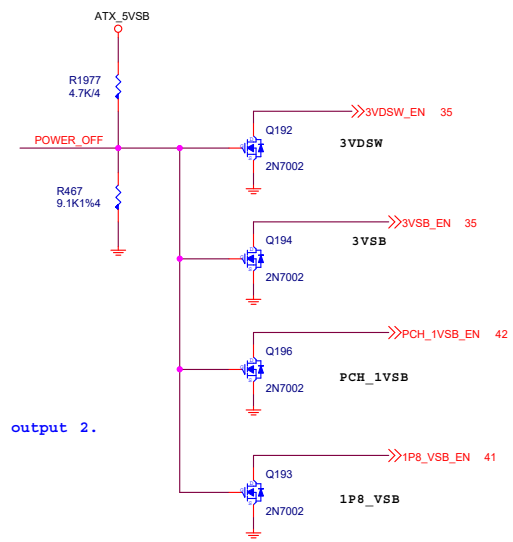
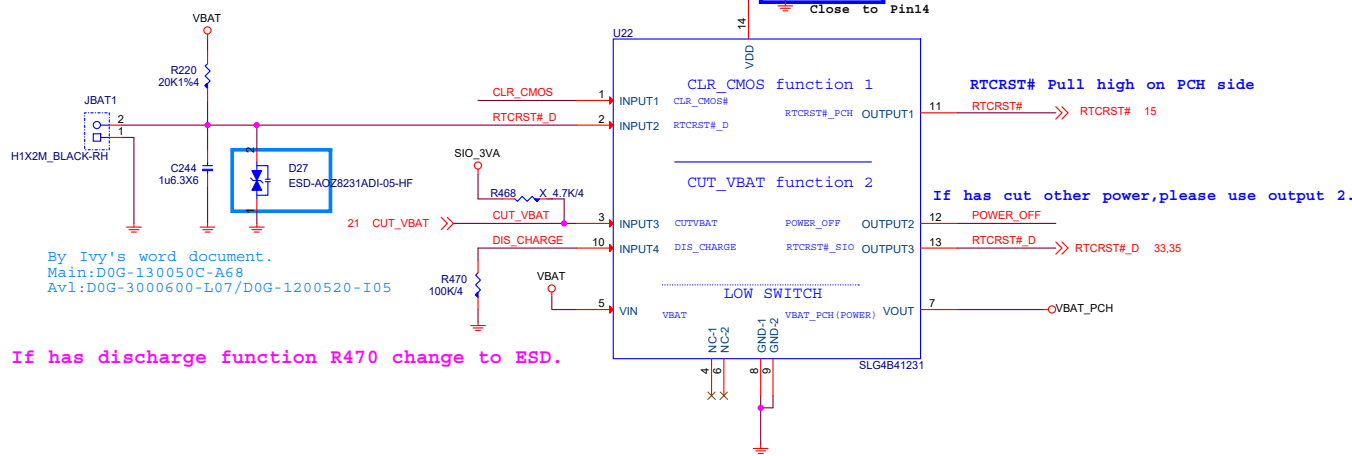
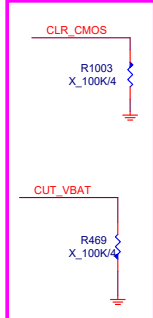
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## Cut VBAT

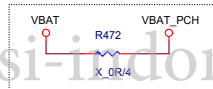
If STUFF R20 Please Check RTCRST# Double Pull High

RTCRST# R223 X\_0R/4 RTCRST#\_D >>> RTCRST#\_D 33,35

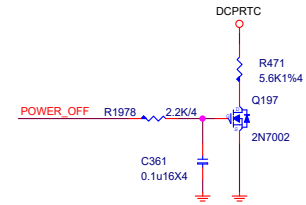
20160629



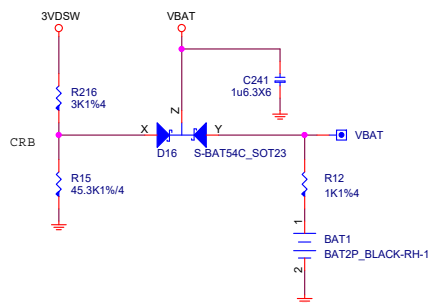
www.teknisi-indonesia.com



Add DCRTC discharge circuit



## VBAT



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

Co-Lay NOT USE U1, R20 STUFF

**MICRO-STAR INT'L CO.,LTD**

**MS-7B33..**

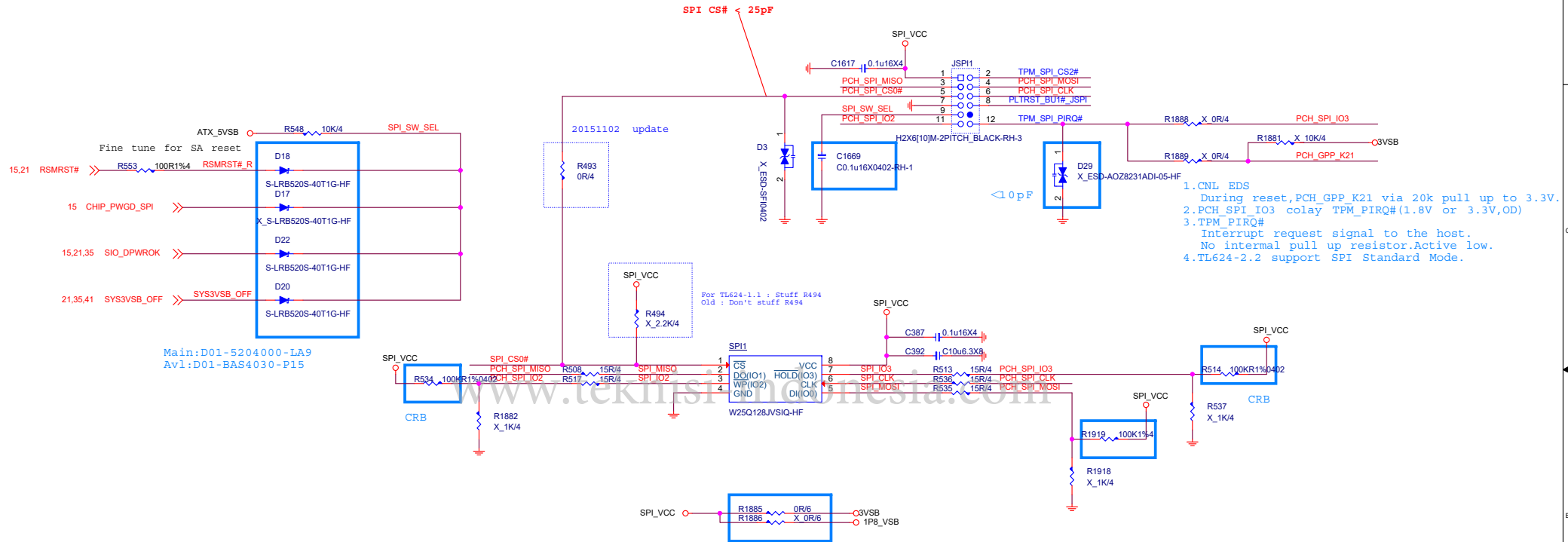
Size	Document	Description	Rev
Custom	CUT_VBAT circuit		10

Date: Wednesday, October 18, 2017

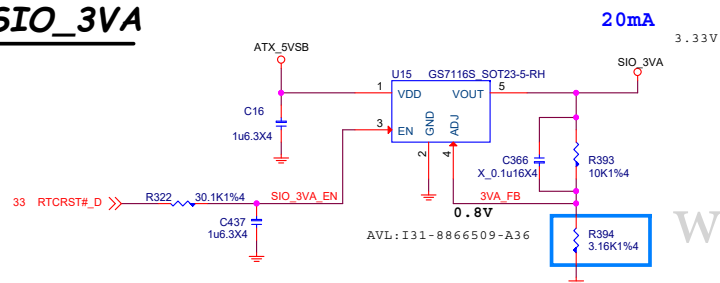
Sheet 33 of 52

15 PCH\_SPI\_MOSI << PCH\_SPI\_MOSI  
 15 PCH\_SPI\_MISO << PCH\_SPI\_MISO  
 15 PCH\_SPI\_CLK << PCH\_SPI\_CLK  
 15 PCH\_SPI\_CS0# << PCH\_SPI\_CS0#  
 15 PCH\_SPI\_IO2 << PCH\_SPI\_IO2  
 15 PCH\_SPI\_IO3 << PCH\_SPI\_IO3

15 TPM\_SPI\_CS2# << TPM\_SPI\_CS2#  
 21 PLTRST\_BU1#\_JSPI >> PLTRST\_BU1#\_JSPI  
 14 PCH\_GPP\_K21 << PCH\_GPP\_K21

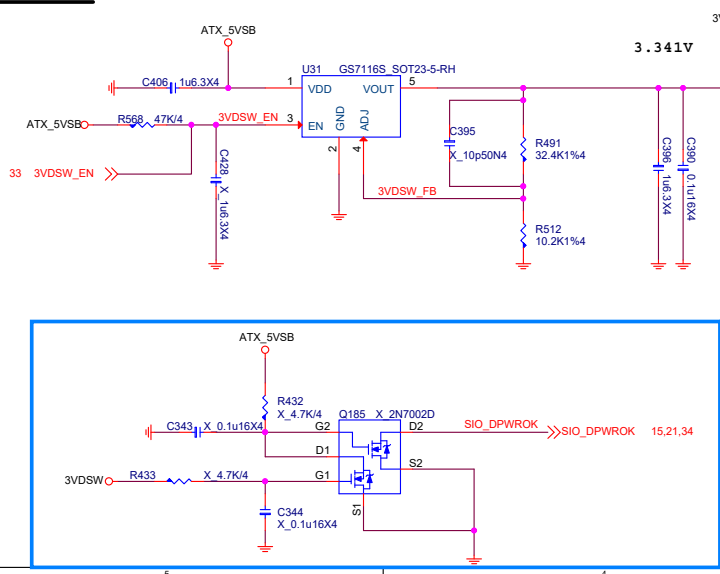


(3A for DDR, 6.6A for USB)

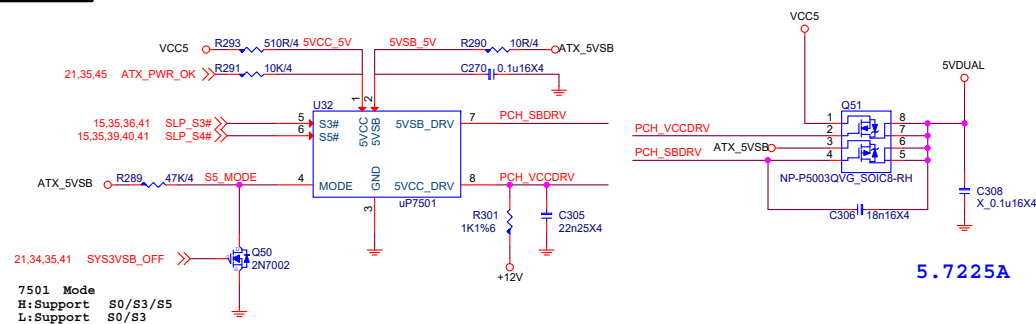


## 3VDSW

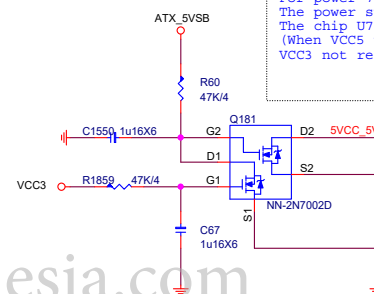
113mA (PCH) + 0.6mA (RTC)



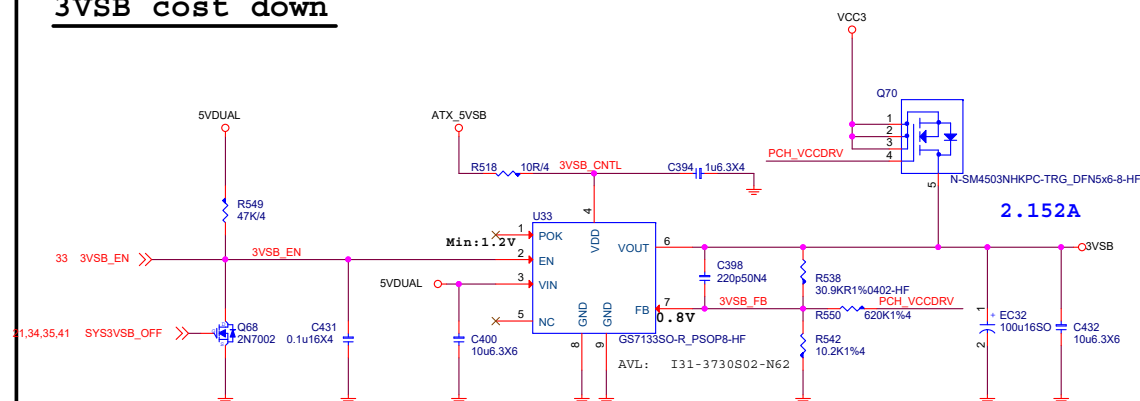
SVDUAL is power source of 1P0SB, 1.8PSB & 3VSB



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



3VSB cost down



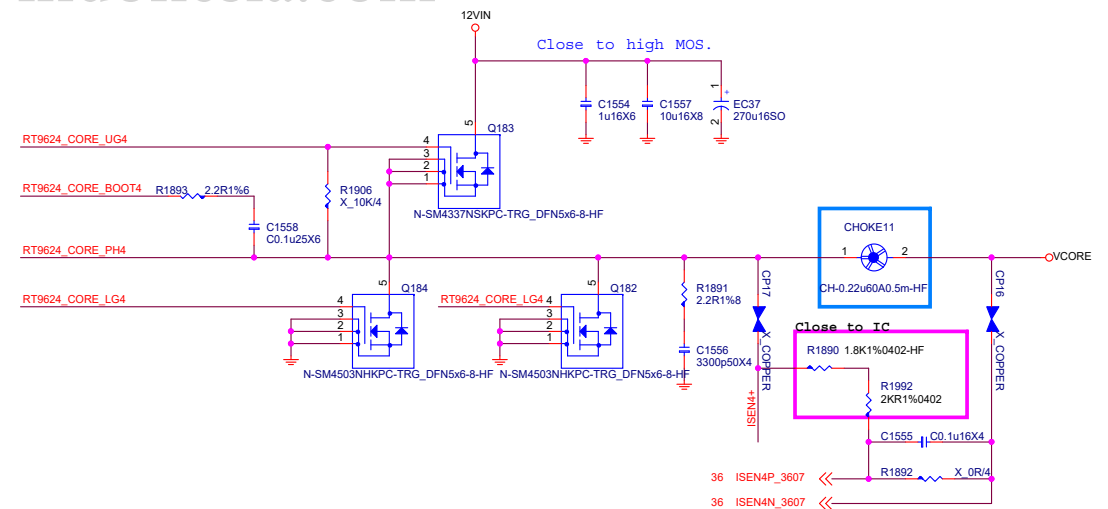
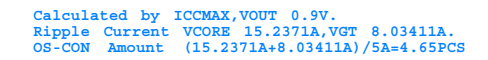
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MS-7B33..

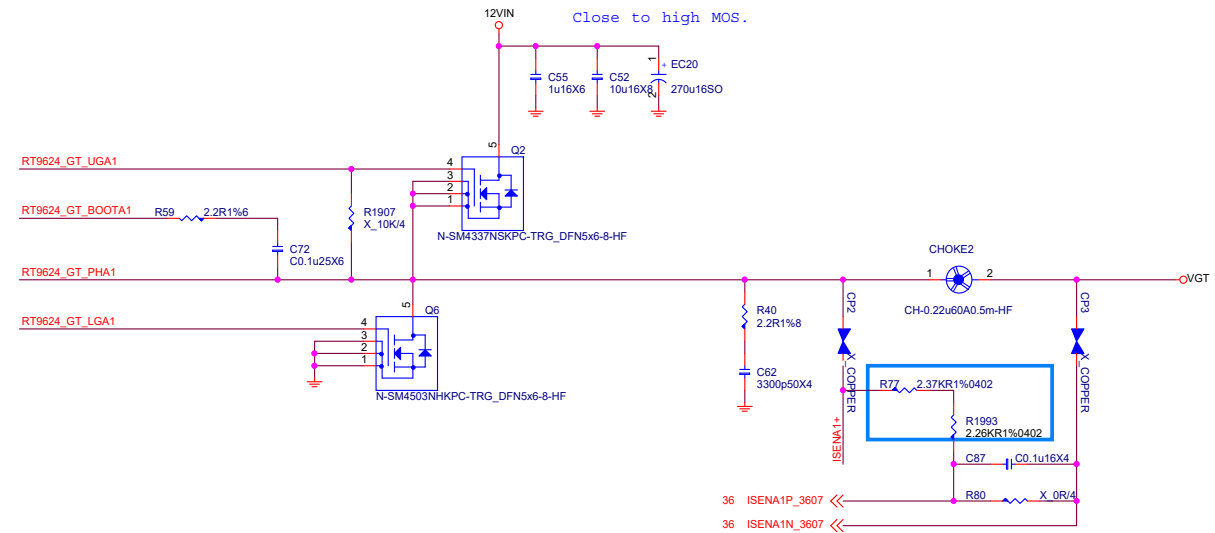
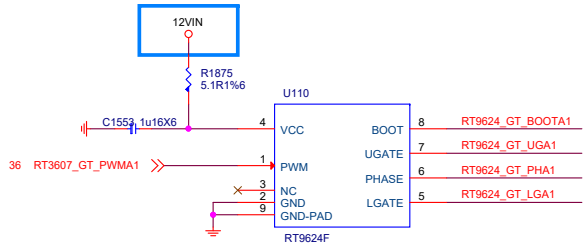
Size Custom	Document Description <b>ACPI CONTROLLER</b>	Rev 10
Date: Wednesday, October 18, 2017		Sheet 35 of 52



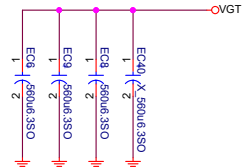
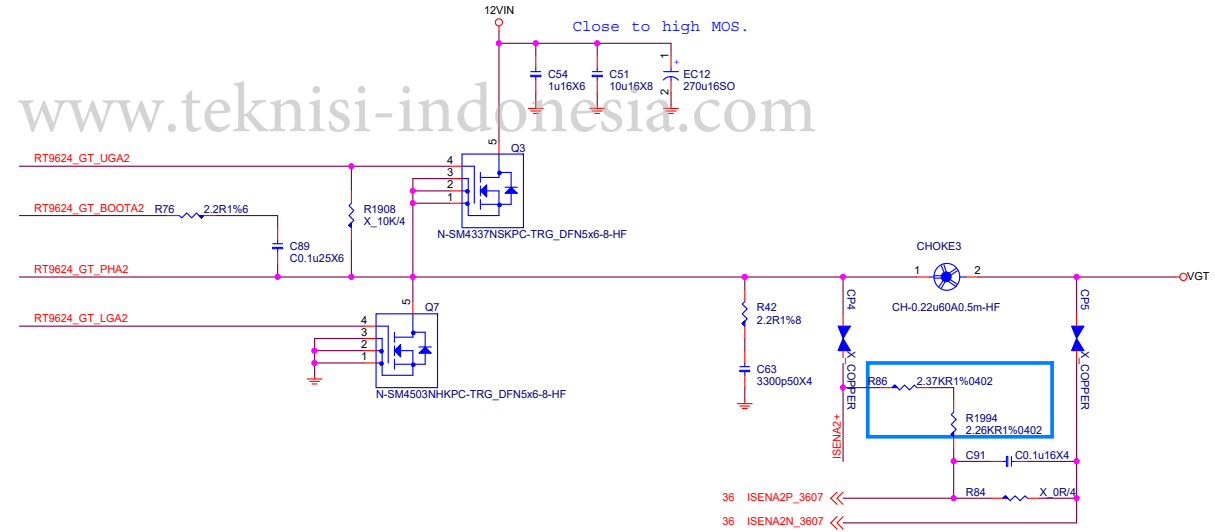
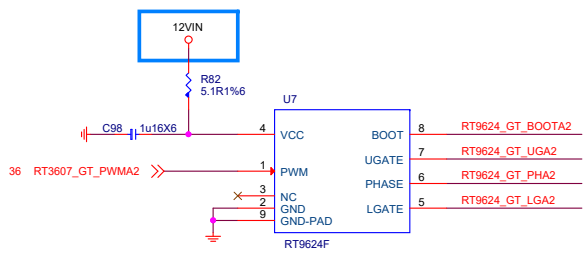




Size Custom	Document Description <b>VCORE(P-PAK) PHASE1-4</b>	Rev 10
Date: Wednesday, October 18, 2017		Sheet 37 of 52



ICCMAX: 45A  
LL: 3.1m ohm



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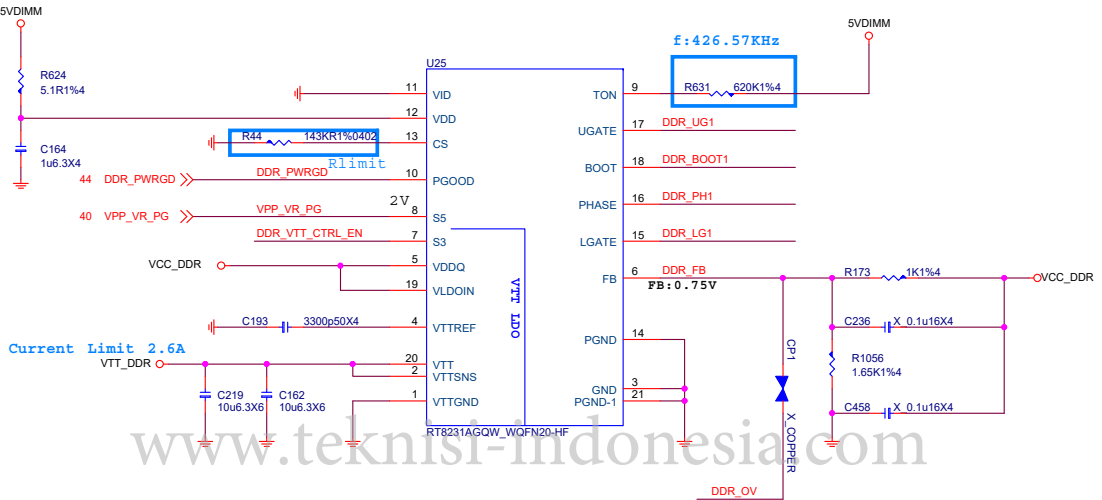
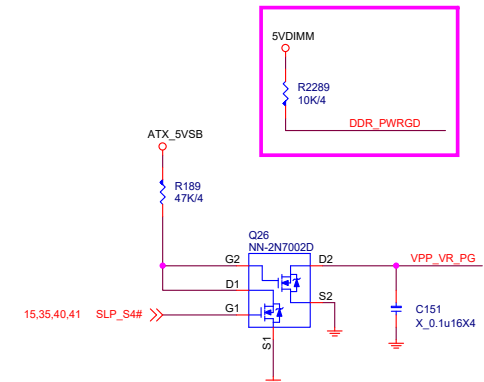
DDR4\_1.2V 3.3A+ 5.85A+0.375A=9.525A

3.3A FOR CPU  
5.85A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR  
D03-4503NOC-ST8  
Current limit= 143K\*5uA/10/5.1mohm)=14.02A

D03-4C02403-O05  
Current limit= 143K\*5uA/10/4mohm)=17.875A

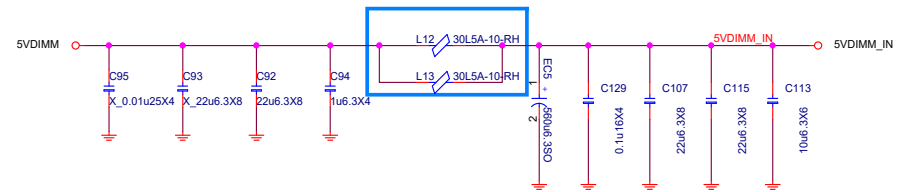
D03-3109M00-U47  
Current limit= 143K\*5uA/10/2.5mohm)=28.6A  
(If UBIQ used finally, Rlimit need to be Calculated again.)

0.4V<=Rlimit \*5uA<=3V



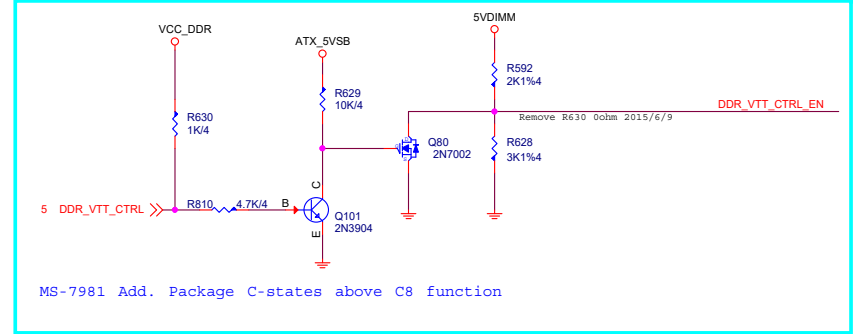
VID	Reference Voltage (V)
H	0.675
L	0.75

Iin=9.525A\*1.2V/0.8/5V=2.8575A  
L02-3008043-M26  
Over 85°C ,Rated Current 1.5A.

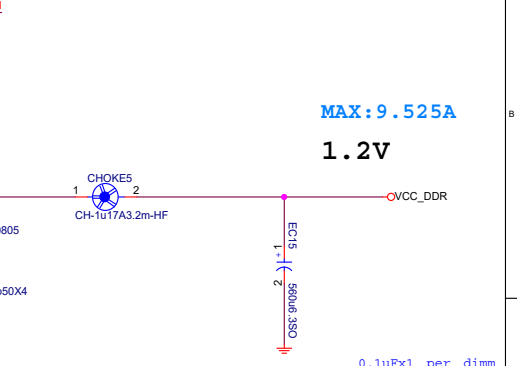
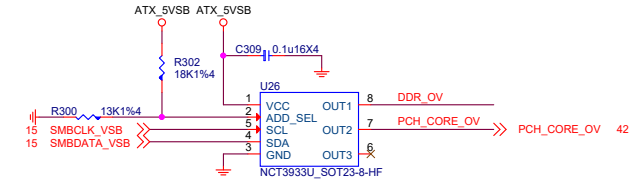


Irms = Iout \* SQRT((Vout/Vin) \* (1-(Vout/Vin)))  
= 9.525 \* 0.427  
= 4.06797A

SLP\_S4# de-assertion to VDDQ ramp down start  
VPP ramp down after VDDQ ramp down



UPI VOLTAGE CONSOLE  
0x26:RH=18K,RL=13K



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Size	Document	Description	Rev
Custom		<b>DDR-RT8231</b>	10

Date: Wednesday, October 18, 2017 | Sheet 39 of 52

**VPP25 Power**  
**2.5V; 1.12A**

AVL:L04-47B7960-C08

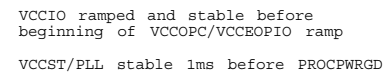
1.12A



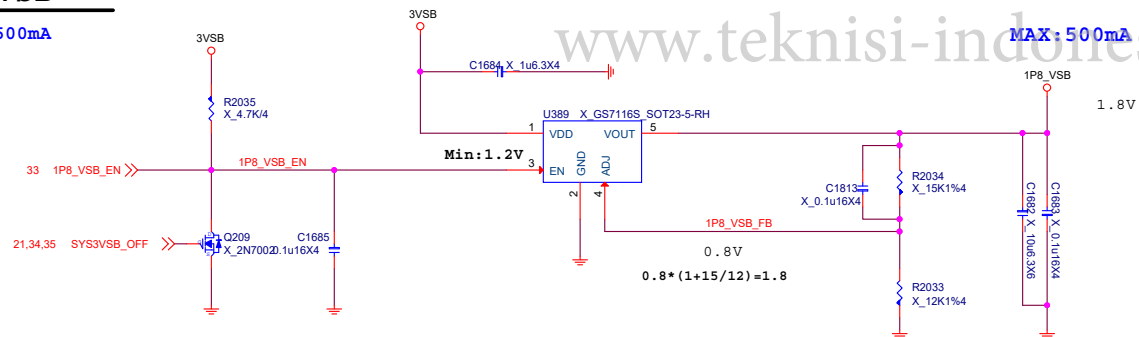
MS-7B33..

Size Custom	Document Description <b>DDR-MP2143-VPP25</b>	Rev 10
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## 1.05V; 250mA



1.8V; 500mA



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Size Custom	Document Description <b>CPU PWR_ST/PLL</b>	Rev 10
Date: Wednesday, October 18, 2017		Sheet 41 of 52

1.05V; 10.743A

$$\text{Current limit} = 11\text{K} * 10\mu\text{A} / 5.1\text{mohm} = 21.568\text{A}$$
$$\text{Current limit} = (11\text{K} \times 10\mu\text{A} / 4\text{mohm}) = 27.5\text{A}$$

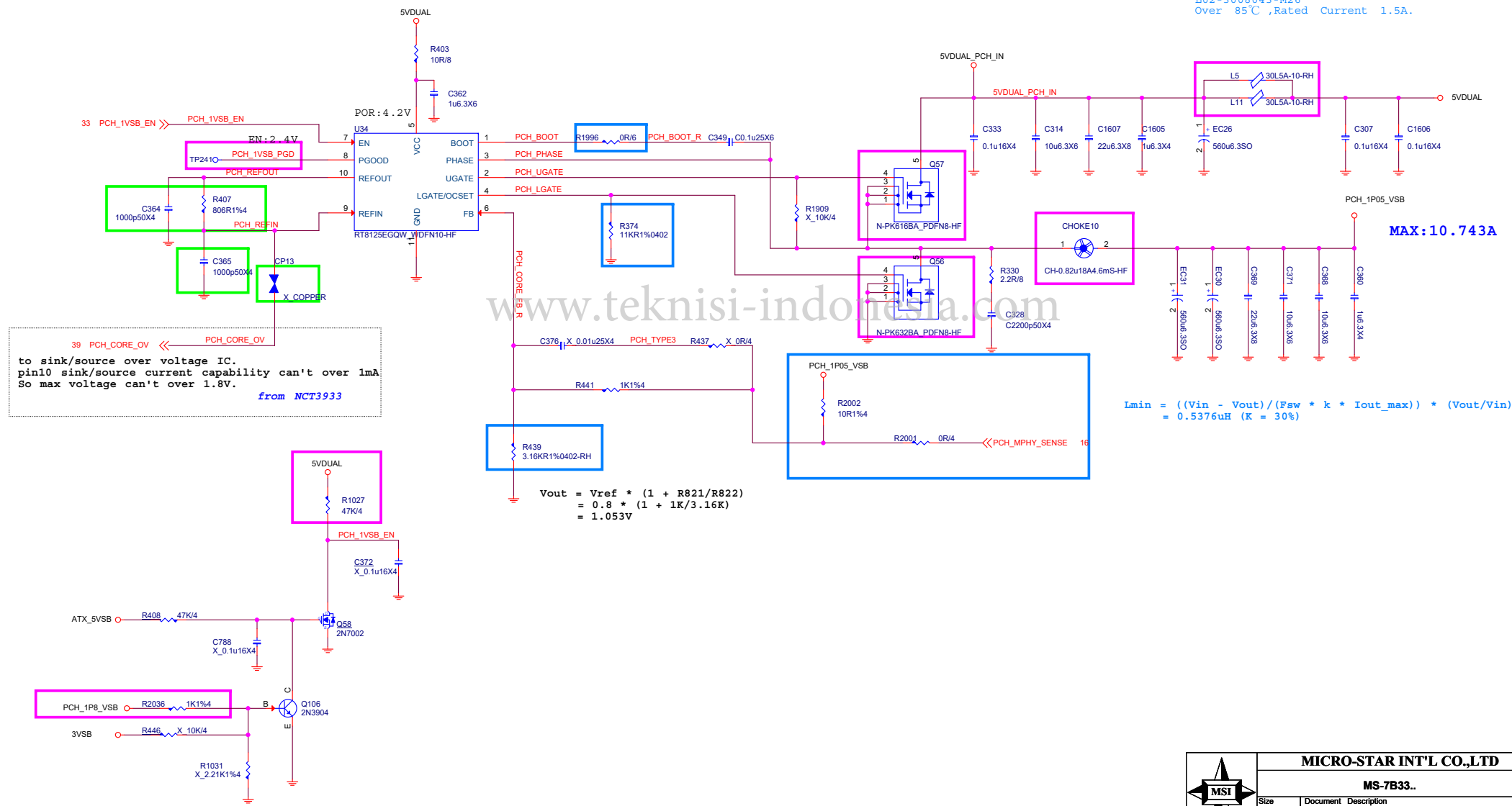
(If ON used finally, Rocset need to be Calculated again.)

$$\text{Current limit} = 11\text{K} * 10\mu\text{A} / 2.5\text{mohm} = 44\text{A}$$

(If UBIQ used finally, Rocset need to be Calculated again.)

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
      =17.143 * 0.407
      =6.977A
```

$I_{in} = 17.143A \times 1.05V / 0.8 / 5V = 4.5A$   
L02-3008043-M26  
Over 85°C, Rated Current 1.5A.

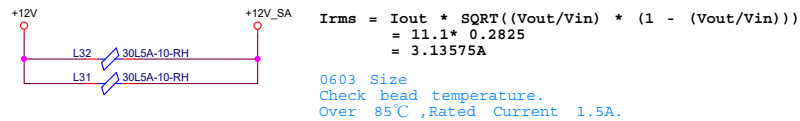


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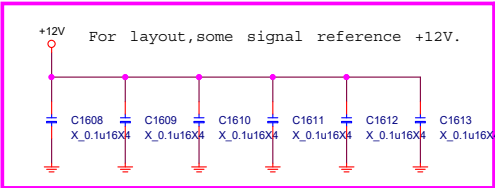
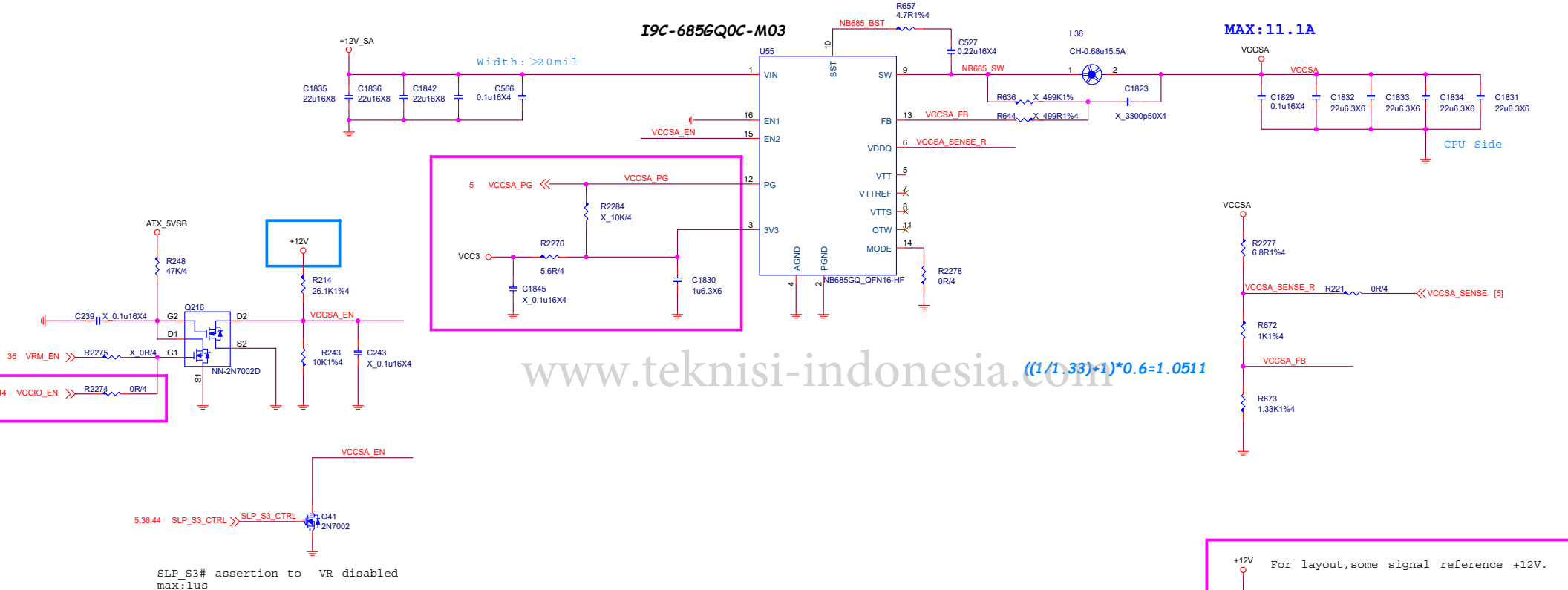
MS-7B33...

Size Custom	Document Description <b>PCH Core power</b>	Rev 10
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SA Power:1.05V,11.1A

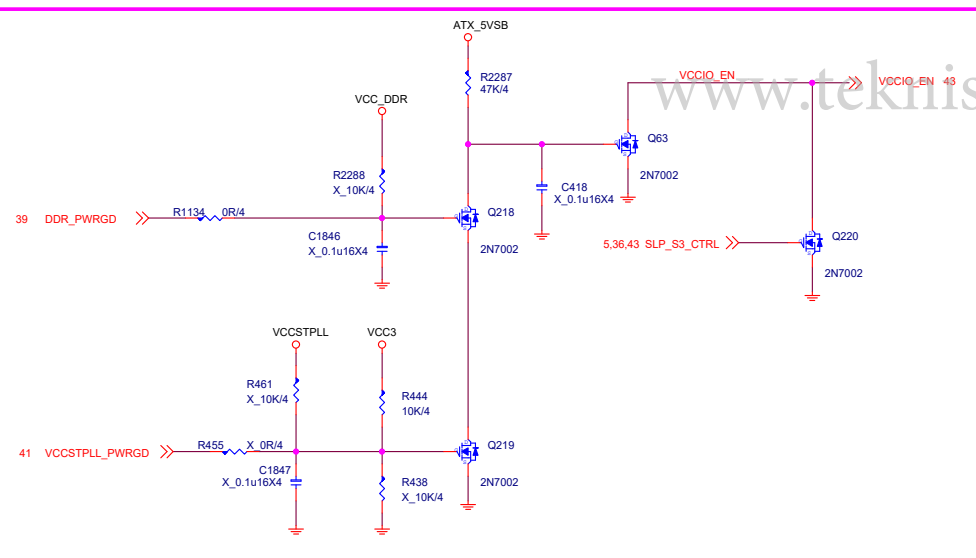
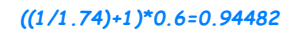


$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$
$$= 0.5914\mu H \text{ (K = 30\%)}$$



0.95V; 6.4A

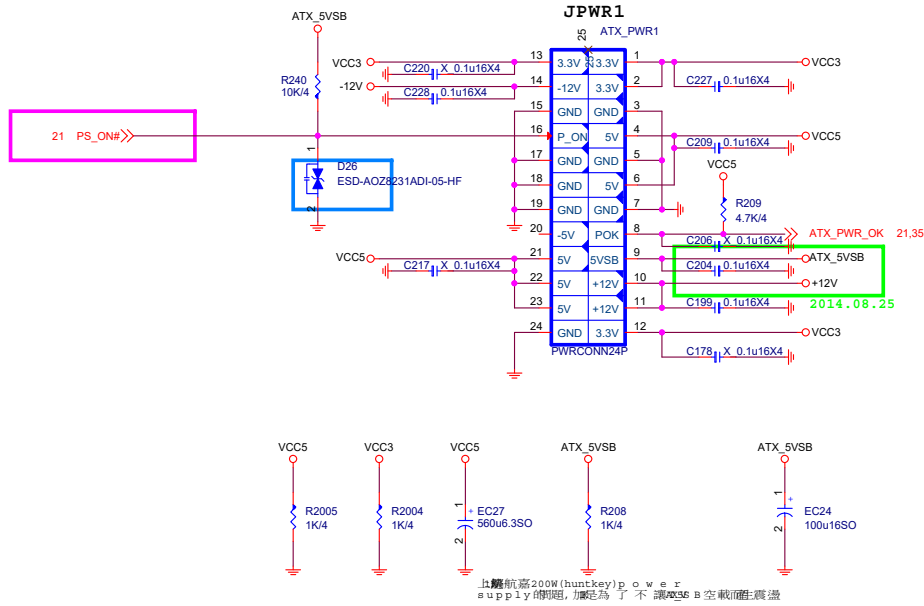
MAX: 6.4A



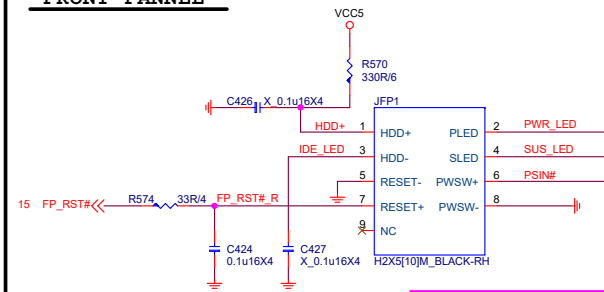


## ATX POWER CONNECTOR

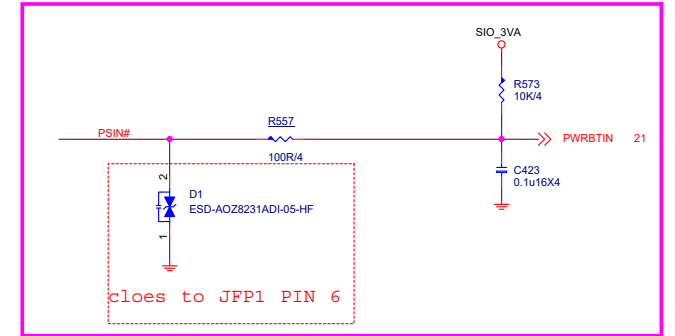
D26:By Ivy's word document.  
Main:D0G-130050C-A68  
Av1:D0G-3000600-L07/D0G-1200520-I05



## FRONT PANNEL



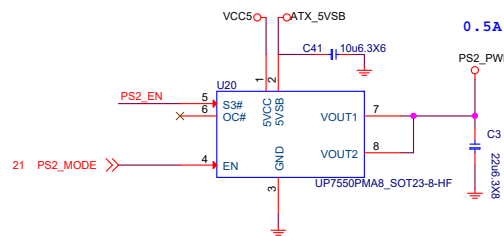
close to SIO



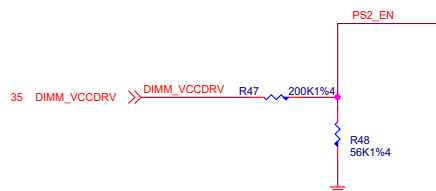
close to JFP1 PIN 6

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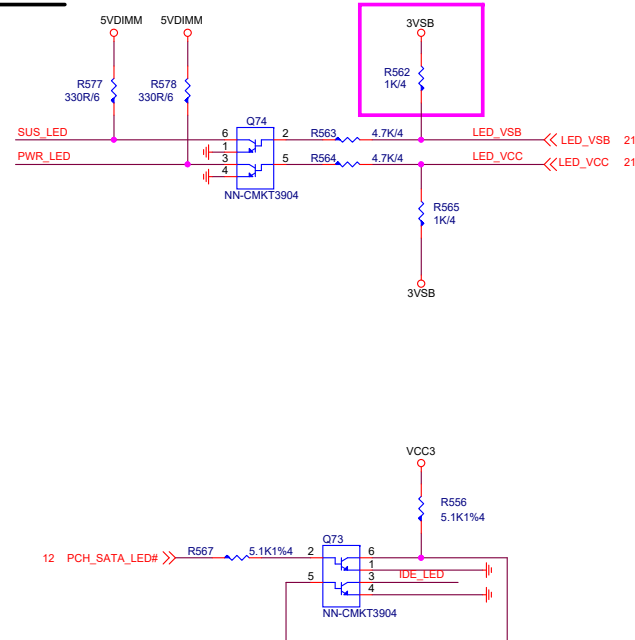
## PS2 POWER



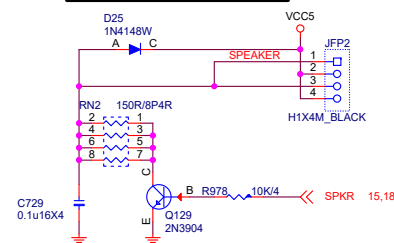
## USB MODE



## LED

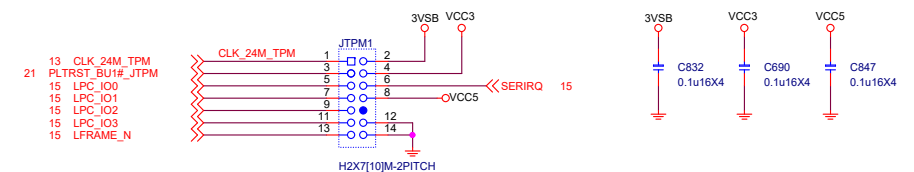


## Speaker Pin Header



## TPM

Don't colay espi debug.

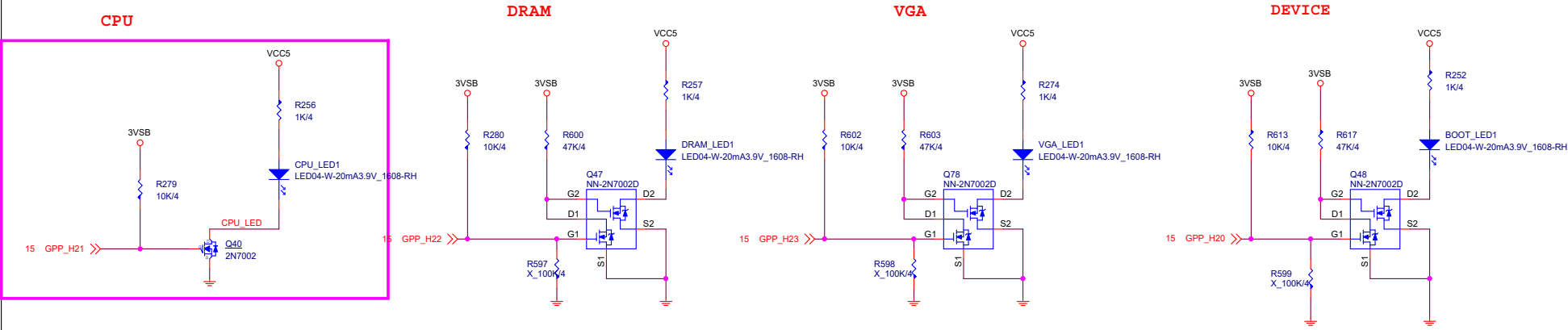


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Size	Document	Description	Rev
Custom	ATX F_Panel/TPM/MSI_LED		10
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DEBUG LED




LED\	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

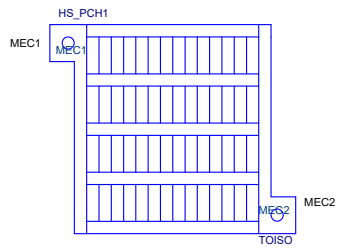
LED  
RED:D0C-040P100-H91  
AVL:D0C-040S500-E07  
  
WHI:D0C-040T200-H91  
AVL:D0C-040S200-E07

- 開機斷電狀態下，3個LED先維持 default 離開機電：
1. 首先進行 CPU check CPU LED 亮，check PASS 後則 CPU LED 滅掉。
  2. 接著依序進行 Memory / memory LED 亮 check PASS 後則 memory LED 滅掉。
  3. VGA 的 check/VGA LED 亮，check PASS 後則 VGA LED 滅掉。
  4. 因此最後正常順利開機後，三個 LED 燈都是滅掉的。(系統重啟 或 其他系統重開機，則 LED 仍按順序動作)

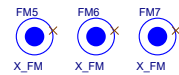
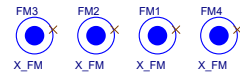
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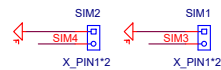
	MICRO-STAR INT'L CO.,LTD		
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Date: Wednesday, October 18, 2017		Sheet 47 of 52	1



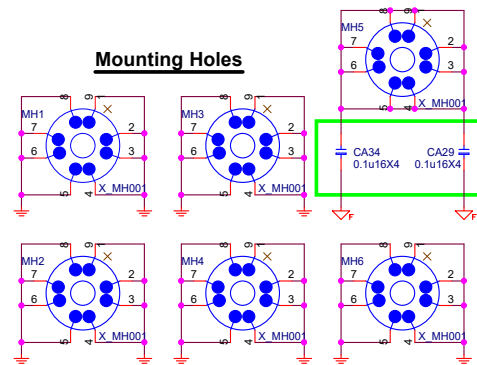
## Optical Fiducial Marks-120



## Simulation



## Mounting Holes



VCC_DDR	VCC_DDR
VTT_DDR	VTT_DDR
5VDIMM	5VDIMM
3VSB	3VSB
3VDSW	3VDSW
PCH_1P05_VSB	PCH_1P05_VSB
PCH_1P8_VSB	PCH_1P8_VSB
VCORE	VCORE
VGT	VGT
VCCSA	VCCSA
VCCSTPLL	VCCSTPLL
VCCIO	VCCIO



7B33\_0A  
PK0-07B330A-G37

## Marketing Name



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